Comparison of etch processes for etching SiO_2 dielectric films

Robert Gunn, Colin Welch, Dean Stephens, Dr. Ligang Deng
Oxford Instruments Plasma Technology

ABSTRACT

This paper compares different aspects of dielectric etching. The two leading techniques for etching dielectric are discussed, namely diode RIE and high density based processes. In the paper we will update the latest results for these techniques and also look at the growing importance of nanoscale etching of dielectric films.

EQUIPMENT

In recent years dielectric etch processes have increasingly been carried out in different types of chambers, depending on the customers etch requirements and budgetary constraints. For dielectric etching where etch rate is not a major driver, with reasonable line widths (typically >1µm), traditional diode-type chambers are used. Where rate is a driver, with smaller line widths (typically <1µm), high-density-plasma systems are used.

Traditional diode, or parallel-plate, plasma chambers are well established in the industry. Parallel-plate systems are classically broken down into two distinct types; these are called Reactive Ion Etch (RIE) or Plasma Etch (PE) systems. Some manufacturers have added magnetic enhancement to these basic systems, to reduce sidewall loses and confine the plasma. Of these two parallel-plate reactors the RIE type system has been the one typically adopted for the etching of dielectric films. In an RIE the plasma is typically generated at radio frequencies with an RF power in the range of a few hundreds of watts, through to kW. For the driving frequency chosen the electrons in the chamber are preferentially accelerated, whereas the ions are driven by the average electrostatic fields. The processed wafer resides on the powered electrode (to enhance ion acceleration). The electron mean free path limits the operating pressure. If the pressure is lowered near the level at which the electron mean free path approaches the gap between the electrodes (generally several cm) the plasma is no longer self-sustaining. A typical RIE arrangement is highlighted in figure 1

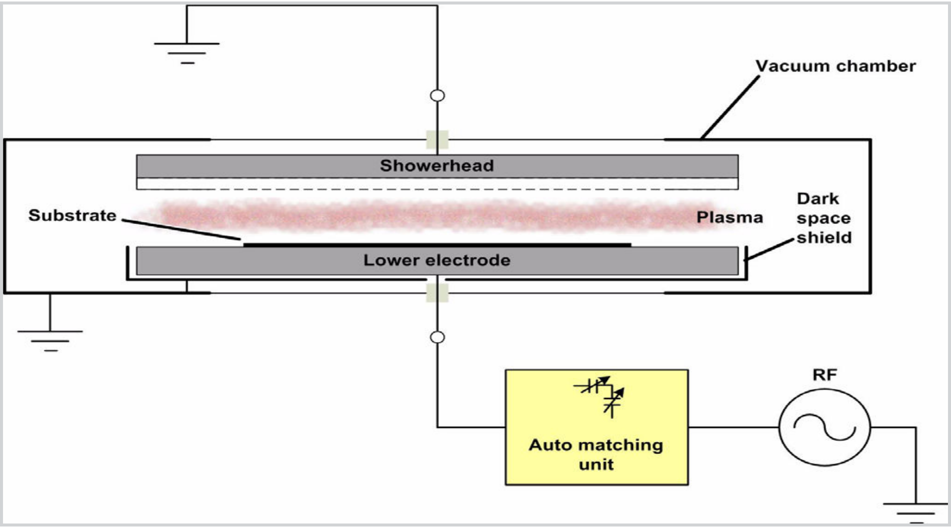


Fig1 *RIE Schematic*

High-density-plasma (HDP) chambers are designed so that the plasma electrons are excited in a direction parallel to the chamber boundaries. The most common HDP source is the inductively coupled plasma (ICP) chamber, which is used by OIPT. In this system the plasma is driven by a magnetic potential set up by a coil wound outside dielectric walls (typical design see figure 2). The direction of the electron current is opposite to that of the coil currents which are, by design, parallel to the chamber surfaces. When the plasma is excited in this manner the electron mean free path can become much greater than the chamber dimensions, and the operating pressure can subsequently be lowered. The lower limit of the pressure is typically dictated by the efficiency of the particular source. In most materials processing plasmas the electron heating is primarily resistive, and the impedance of the plasma scales with the density of neutrals available for inelastic collisions. As the impedance (pressure) is lowered so is the ability of the source to drive the plasma.

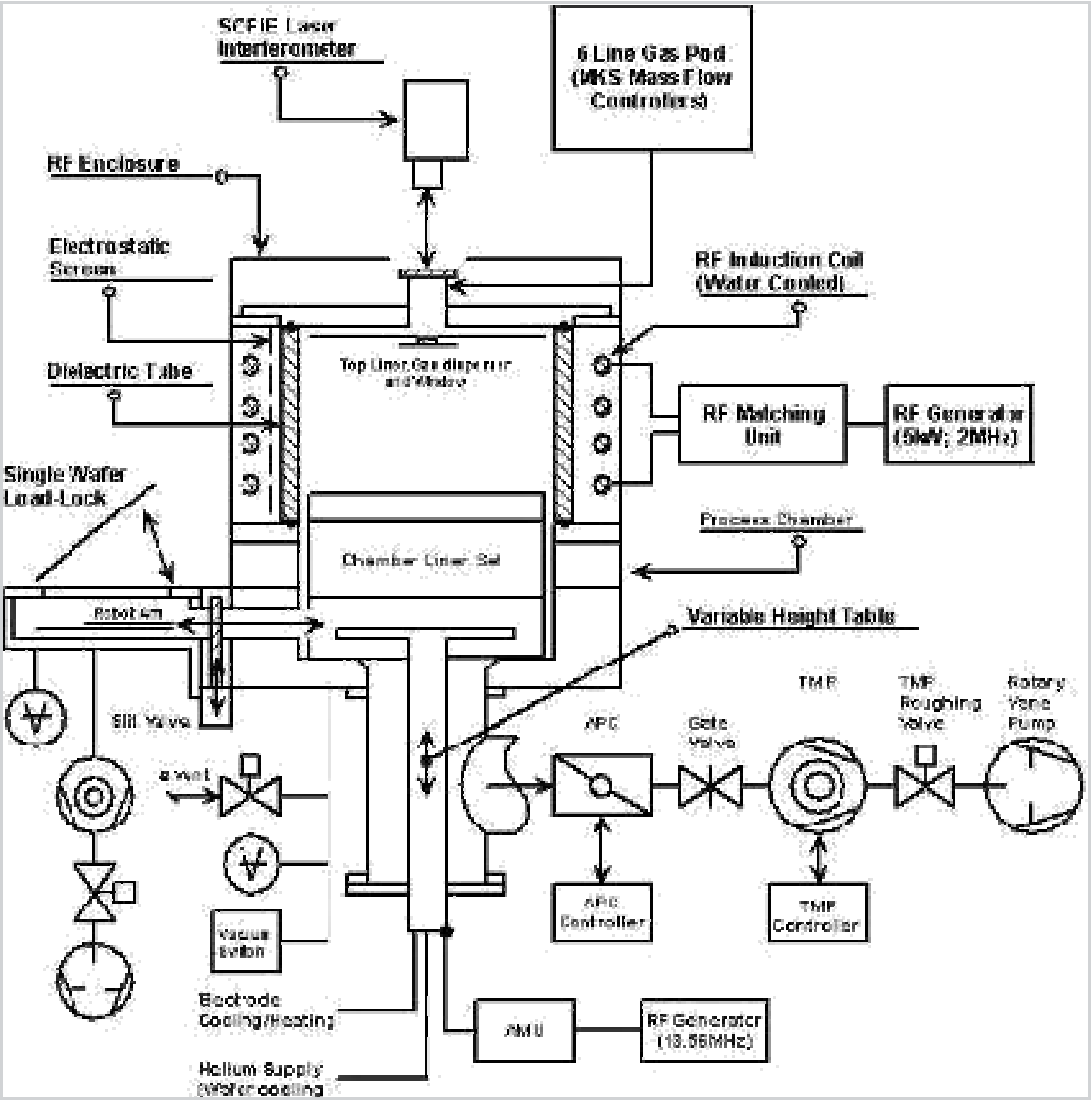


__Figure 2__ OIPT 300mm compatible source

High-density sources allow the wafer platen to be powered independently of the source, providing significant decoupling between the ion energy (wafer bias) and the ion flux (plasma density primarily driven by source power). In a plasma-etching environment the anisotropy is provided by the acceleration of ions through the plasma sheaths, in a direction normal to the wafer surface.

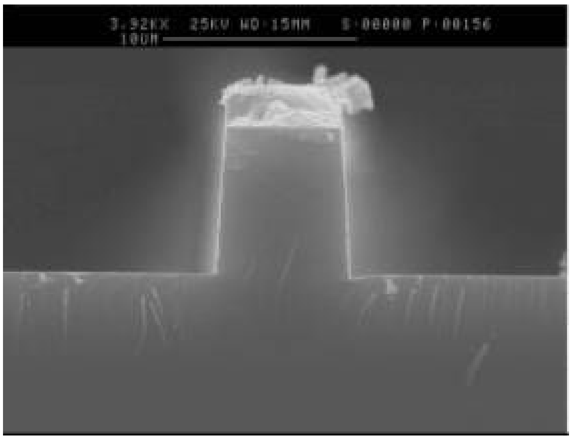
The anisotropic component is maximized when the incoming ion flux is as normal as possible to the surface. The isotropic component of the incoming ion flux is either thermal (typically less than 0.1 eV, compared to several hundred eV for the sheath voltage), or caused by collisions of the ions in the sheaths with neutrals (either elastic or charge-exchange). Operation in a lower-pressure/higher-density regime provides much thinner and less collisional sheaths, making it possible to obtain a more anisotropic etching component.

The primary processing advantages of ICP for dielectric etching are better CD control, higher etching rates, higher aspect ratios and an improved processing window.

The patterning of dielectrics, especially silicon dioxide, is inherent in the manufacture of modern semiconductor devices, optical waveguides, RF ID's, nanoimprint etc. Because of higher bond energies dielectric etching requires aggressive, ion-enhanced, fluorine-based plasma chemical systems. Vertical profiles are achieved by sidewall passivation, typically by introducing a carbon-containing fluorine species to the plasma (e.g., CF_4, CHF_3, C_4F_8). High ion-bombardment energies are required to remove this polymer layer from the oxide, as well as to mix the reactive species into the oxide surface to form SiFx products.

Dielectric etching applications typically rely on the competing influences of polymer deposition and reactive ion etching to achieve vertical profiles, as well as etch-stopping on underlying layers. As hard-mask open-feature sizes shrink to 0.18 µm or less, for nanoimprint applications, aspect ratios are increasing to 4:1 or more. The ion and radical flux to the bottom of these features is reduced, owing to collisions with the feature sidewalls and other species present in the feature. Etch products (e.g., $Si_xF_yO_z$ and C_xF_y) cannot diffuse out of these features readily, resulting in excessive polymerization near the bottom of the feature which creates highly tapered features and poor mask transfer.

Traditional RIE type processes are typically based around CF_4/CHF_3; usually combined with either O_2, He, Ar or a permutation. Because the ion energy can't be independently controlled increasing the RF power will eventually lead to excessive photoresist damage. This limits the etch rate that can be achieved, which can be alleviated to some degree by using better cooling (utilising clamping and supplying He to the backside of the wafer). For the process performed in SEM1 the etch rate can be doubled from 35nm to 70nm by using such a method. Another way to increase the throughput is to increase batch size. This is feasible for smaller wafer sizes, up to 100mm, but for 150mm and above the system size becomes excessive, with the added issues of across batch uniformity etc. Diode chambers, also, are run at pressures usually of the order of 10's of mT, in order to sustain the plasma (see earlier), this reduces the anisotropy and aspect ratios that can be etched.



SEM 1 *RIE Waveguide etch*

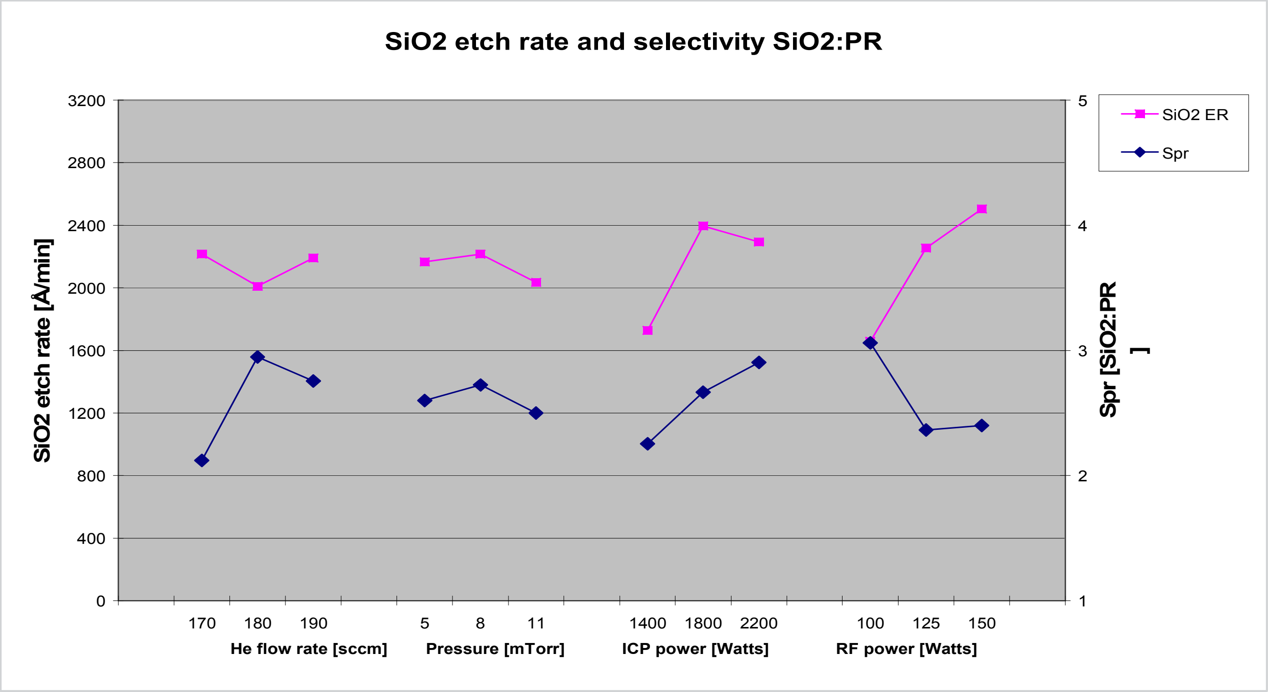
OIPT have developed high-density systems to address many of the issues related to etch rate, anisotropy and aspect ratio dependence. In a high-density system the operating pressure can be much lower (10mTorr or less), and the diffusivity and mobility of the reactive species correspondingly higher. In addition the ion flux is independently tuneable by the source power, so that the total ion flux can be increased without as much of an increase in the ion energy, potentially reducing resist damage.

Employing traditional chemical systems (e.g., CF_4/CHF_3) in an ICP chamber may lead to excessive resist loss/damage.

This occurs because the higher ion flux removes too much of the polymer protecting the resist. The greater dissociation efficiency, and high ion flux of high-density-plasma sources, permits the use of a more highly polymerizing feed gas (e.g., C_4F_8). Because of their lower operating pressures (i.e. increased species diffusivities) chamber wall conditions play a more important role in ICP chambers. For example, to control polymer build-up the chamber wall temperature is regulated, pumping speed is maximised, plus periodic plasma cleaning steps are used prior to processing a wafer.

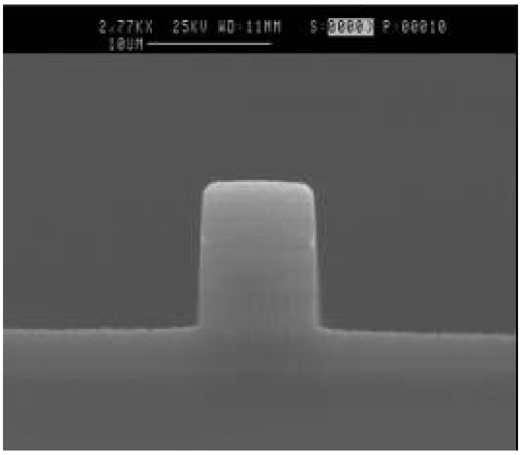
OIPT's ICP based silicon dioxide etching system is based on C_4F_8 combined with O_2 and/or noble gas He. Since C_4F_8 is a strained ring molecule dissociation products are thought to consist of high levels of CFx (x $\leq$2) polymer precursors.

A simple L9 Taguchi matrix has been run at OIPT to ascertain the influences of the process parameters such as flow, ICP power etc., on the process. The trends are shown in Graph1

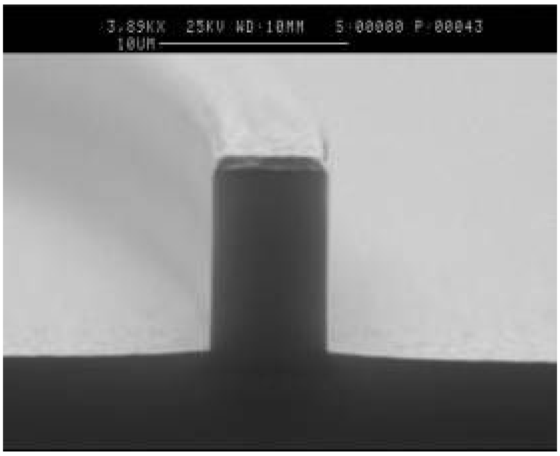


Graph 1

Utilising this information similar structures to those seen in SEM 1 have been etched, at >3times the etch rate and with straighter sidewalls see SEM 2 and SEM 3

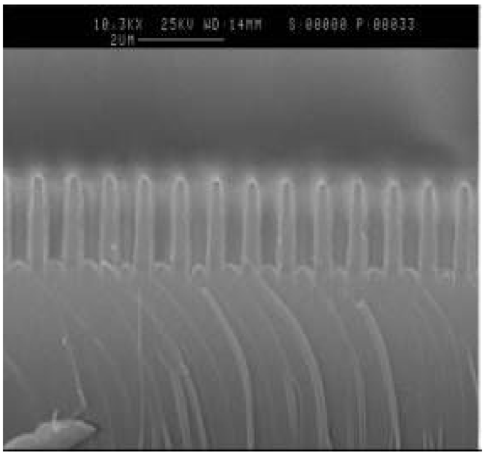


SEM 2

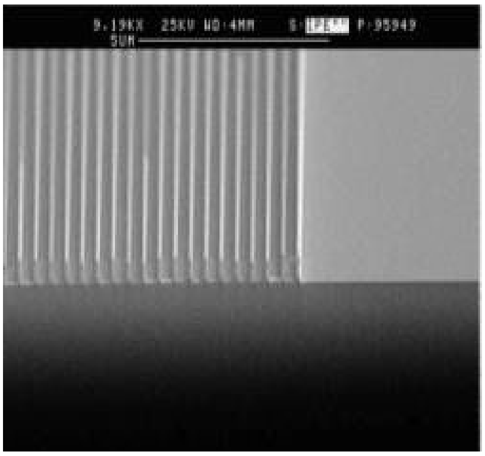


SEM 3

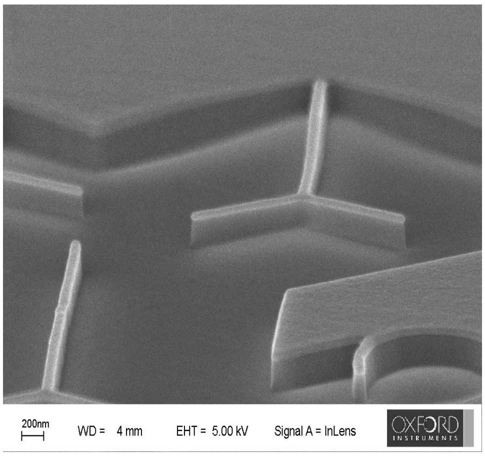
Using an HDP source such as ICP, which operates at low pressures, opens up the possibility of etching nanoscale features which are not possible in a traditional diode system. This requires precise control of the ion flux to the surface to control the polymerisation - too low, and the possibility is that the etch profile will taper or it will stop completely. Working closely with nano-centres such as those at Cornell and LBNL, OIPT has developed a range of processes capable of etching structures with line widths of the order of 100nm, examples of these are shown in SEMS 4, 5 and 6



SEM 4



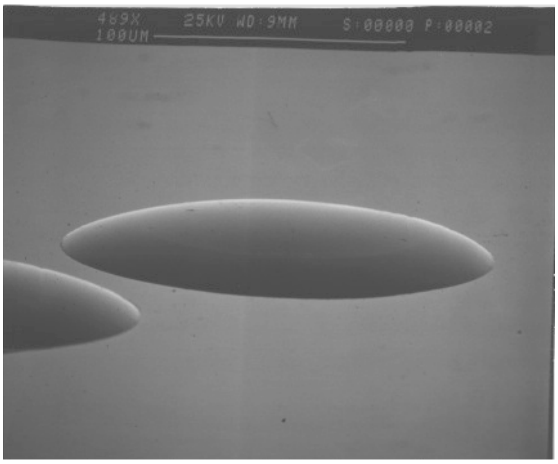
SEM 5



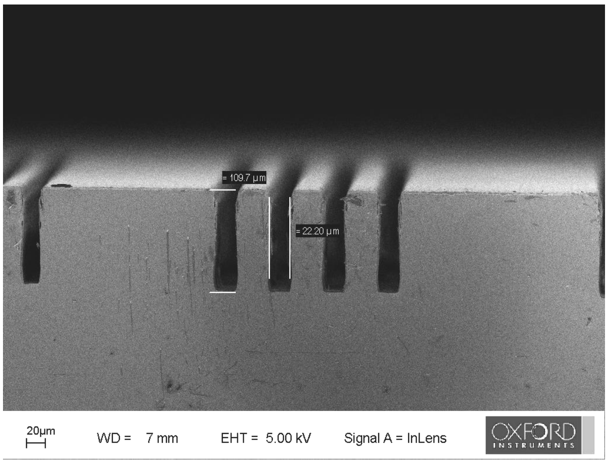
SEM 6

Some semiconductor equipment manufacturers have reported improved selectivity with the addition of hydrogen to the C_4F_8-based system. This hydrogen inclusion generates far greater levels of C_xF_y polymer compared with systems operating with none. OIPT have found that using such a process leads to excessive polymer build up in the reactor, even if sophisticated chamber heating is utilised. This results in more frequent plasma cleaning, plus the possibility of more mechanical cleans - decreasing productive process time along with increasing cost of ownership. OIPT have found that by achieving the correct balance of process and hardware, whilst excluding the use of H_2, that in excess of 1000 wafer μm can be etched prior to a plasma clean becoming necessary.

One process that shows the control that can be achieved, for dielectric etching, in the OIPT ICP system is the etching of micro-lenses into a SiO_2 based material, such as quartz or glass. Control of the ion flux, plus gas chemistry, is required to achieve the desired micro-lens shape in the substrate material, as the carbon loading changes with time. SEM7 shows an example of a perfectly etched micro-lens.

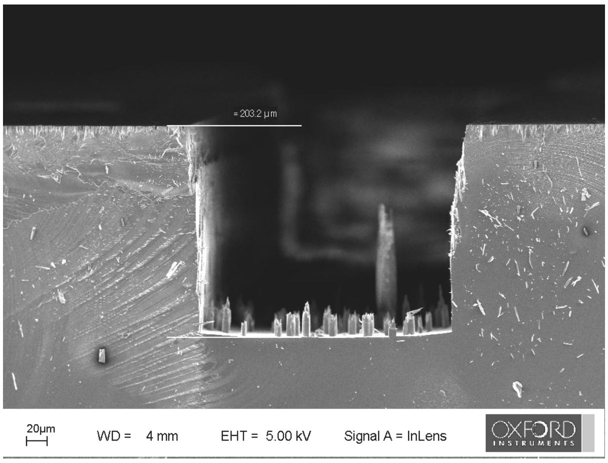


SEM 7



SEM 8

Recent developments have shown that a trend towards deeper dielectric etches, of the order of >100µm, are being required. Normal photo-resist masks can't be used to etch to this depth so metal masks, such as Cr and Ni, are being used which can offer selectivity's of >100:1. This gives more latitude in the process chemistry that can be used, but control of the ion flux is still paramount. Too high, and the mask will be eroded due to sputtering before the desired depth is reached. SEM's 8 and 9 show a deep quartz etch utilising a Cr mask. For SEM9 there was a masking issue which left residue, but it shows the capability to etch to substantial depths.



SEM 9

Conclusion

Both the diode and ICP processes, for dielectric etching, discussed have evolved over the years - in terms of hardware and process. The ICP based process offers higher etch rates, with better CD and anisotropy control, along with higher aspect ratios etc. Achieving these improvements requires the use of larger turbomolecular pumps, which come at a cost, but the advantages of the higher rates more than compensate for this. Also, by utilising these larger pumps and independent ion flux control, the possibility of etching nanoscale features is opened up.

The diode system does offer a cost effective solution for etching of dielectrics with larger linewidths, but at a much slower rate, and cannot be used for etching of nanoscale features.