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Inductively coupled plasma chemical vapour deposition (ICP-CVD)

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Introduction

A wide range of insulating thin films are used in modern VLSI circuits providing electrical isolation between conducting regions within a device, and as a final capping passivation layer. Silicon dioxide, silicon nitride and oxynitrides are widely used. Various deposition methods are available dependant on deposition temperature. Atmospheric pressure chemical vapour deposition and low pressure chemical vapour deposition methods typically require high temperatures in the region of >400 °C whereas the use of plasma enhanced chemical vapour deposition (PECVD) typically requires deposition temperatures of <400 °C.

Considerable interest has been directed towards the ability to deposit high density dielectric films at even lower temperatures (<150 °C), especially in temperature-sensitive devices such as organic LEDs. By using the ICP-CVD technique, Oxford Instruments have developed a deposition process in which high quality films can be deposited with high density plasma, low deposition pressures and temperatures.

Experimental

Low temperature depositions are typically achieved by using plasma in which the gases react in a glow discharge. This discharge ionizes the gases, creating active species that react at the wafer surface. The most common method is a parallel plate reactor in which the sample sits on a grounded bottom electrode and radio frequency voltage is applied to the top electrode. This creates a glow discharge between the two plates and the gases flow radially through the discharge. Typically the bottom electrode is heated to $100-400$ °C and this method is usually referred to Plasma enhanced chemical vapour deposition (PECVD). However in order to deposit high density films dielectric films at even lower temperatures (<100 °C) OIPT have developed a high-density-plasma (HDP) source in which the plasma electrons are excited in a direction parallel to the chamber boundaries.

The HDP source used is the inductively coupled plasma (ICP) chamber, in which the plasma is driven by a magnetic potential set up by a coil wound outside dielectric walls (typical design see figure 1). The direction of the electron current is opposite to that of the coil currents which are, by design, parallel to the chamber surfaces. When the plasma is excited in this manner the operating pressure can subsequently be lowered. The lower limit of the pressure is typically dictated by the efficiency of the particular source. In most materials processing plasmas the electron heating is primarily resistive, and the impedance of the plasma scales with the density of neutrals available for inelastic collisions. As the impedance (pressure) is lowered so is the ability of the source to drive the plasma.

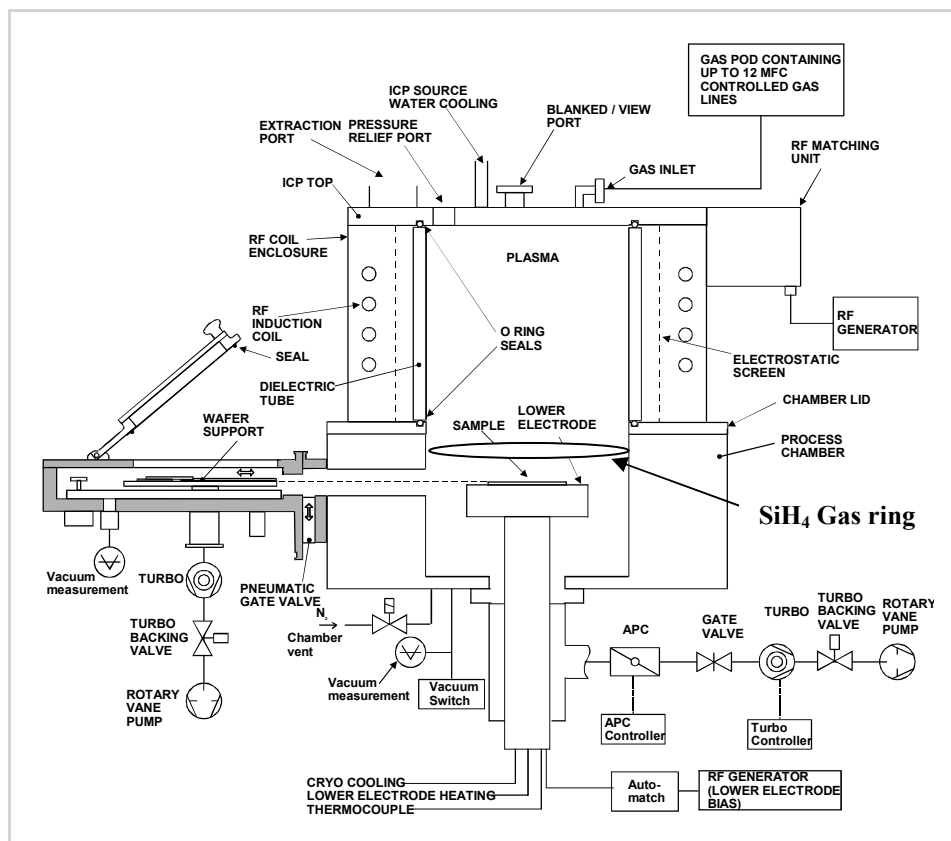


Figure 1: OIPT ICP-CVD system

For plasma depositions there are additional system features:-

- The inductively coupled coil is connected to a 13.56 MHz, 3.0kW RF generator via a matching unit.
- The ICP coil power controls the dissociation of the plasma and the density of the incident ions in the chamber.
- The lower electrode is separately powered by another 13.56 MHz 300W generator, which allows independent control of the bias voltage, i.e. the energy of the ions on the sample.
- In order to reduce the plasma-induced damage during deposition processes and the stress level in deposited films, the ICP-CVD system has been operated in a purely "ICP" mode by applying RF power (100 to 2000W) to only the ICP coil, but no RF power on the lower electrode.
- Helium pressure was applied to the back of the wafers to provide good thermal contact between chuck and wafer.
- The system has precise control of substrate temperature from -150°C to $+400^{\circ}\text{C}$ by using electrical heater and liquid nitrogen. This wide temperature range is important for the advanced plasma deposition processes of different substrate materials.
- Pure silane (100% SiH_4) is introduced into the deposition chamber through a gas distribution ring. Other gases such as N_2 and N_2O are introduced into the ICP source chamber
- Automatic pressure controller (APC) is used to control the pressure (2 to 20mTorr).

A summary of the ICP-CVD system configurations are shown in table 1 below:

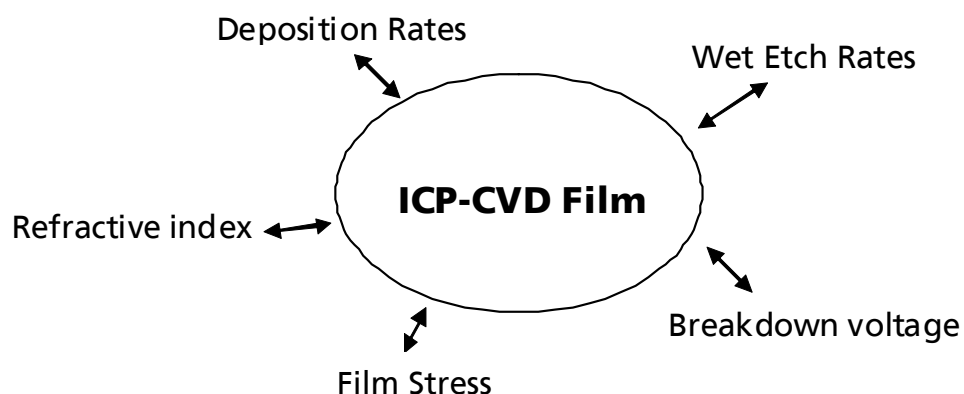
Feature	System 80Plus	System100	System100	System133
ICP	ICP65	ICP-CVD180	ICP-CVD380	ICP-CVD380
Electrode size	240mm	240mm	240mm	Up to 330mm
Loading	Open Load	Load locked	Load locked	Load locked
Substrates	50mm wafers	150mm with carriers options available for multi-wafers or small pieces	200mm with carriers options available for multi-wafers or small pieces	Up to 300mm with carriers options available for multi-wafers or small pieces
Dopants	No	Various dopants available which include PH ₃ , B ₂ H ₆ , GeH ₄	Various dopants available which include PH ₃ , B ₂ H ₆ , GeH ₄	Various dopants available which include PH ₃ , B ₂ H ₆ , GeH ₄
Liquid Precursors	No	No	No	No
MFC controlled gaslines	8 or 12 line gas box available	8 or 12 line gas box available	8 or 12 line gas box available	8 or 12 line gas box available
Typical Wafer stage temperature range	20°C to 400°C	0°C to 400°C	0°C to 400°C	0°C to 400°C
Insitu plasma clean	Yes	Yes	Yes	Yes

Table 1: ICP-CVD Tools from Oxford Instruments

Process Results

ICPCVD can be used to deposit several materials e.g. SiO₂, SiN_x, SiO_xN_y, a-Si and SiC. In this paper we will concentrate mainly on the ability to deposit high quality SiO₂ and SiN films at substrate temperature as low as 20 °C. In an ICP-CVD chamber the silicon dioxide films are deposited by reacting silane which is introduced through the gas distribution ring and nitrous oxide which is introduced through the ICP source. Additionally silicon nitride films are deposited using silane which is introduced through the gas distribution ring and nitrogen which is introduced through the source. Alternatively ammonia can also be used to deposit silicon nitride but the use of nitrogen results in a higher quality film which will be explained in more detail later.

Typical process parameters which are discussed here include deposition rate, film thickness uniformity, refractive index, film stress, wet etch rates, and breakdown voltage.



Deposition Rate

Traditionally ICP-CVD processes results in lower deposition rates than PECVD films. Typical deposition rates for silicon oxide and silicon nitride are >8nm/min but higher deposition rates are now possible in which results can be seen in the next section. In a similar way to conventional parallel plate deposition methods many process parameters can be adjusted in order to control the process. Figure 2 and 3 below show typical deposition rate trends with different process parameters.

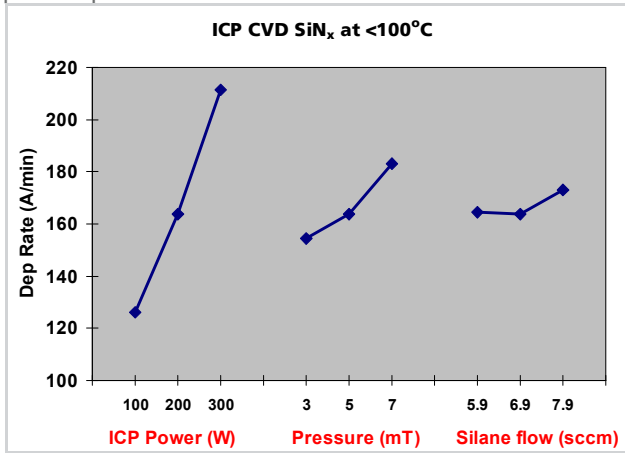


Figure 2: Effect of ICP power, pressure and silane flow on ICP-CVD Si_xN_y deposition rate

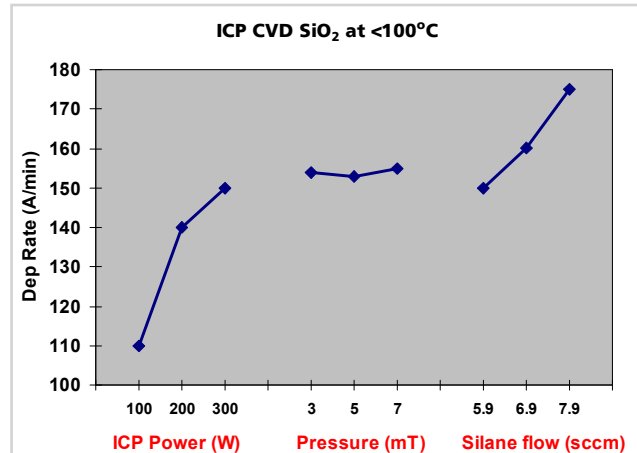


Figure 3: Effect of ICP power, pressure and silane flow on ICP-CVD SiO₂ deposition rate

Refractive Index

The refractive index can be controlled by varying the ratio of the Si:N for silicon nitride deposition or Si:O for the silicon oxide deposition. Silicon nitride films have typical refractive index of 2.00 (at 633nm) although this value can be adjusted by varying the silane and nitrogen flows. Silicon dioxide films have typical refractive index of 1.46. The RI value can be adjusted by varying the silane and nitrous oxide flows. In both films a higher refractive index value usually indicates a silicon rich film. Figure 4 and 5 below show the relationships of refractive index with different gas flow ratios.

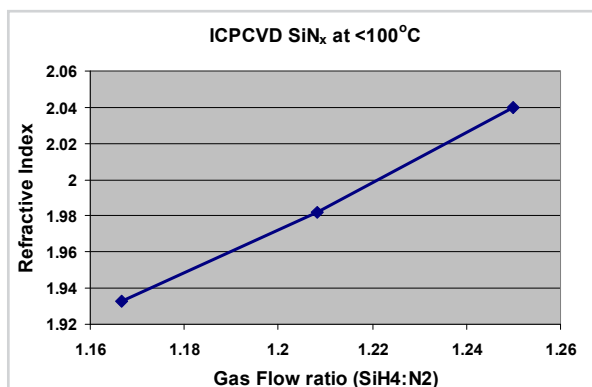


Figure 4: Variation of refractive Index with SiH₄:N₂ gas ratio

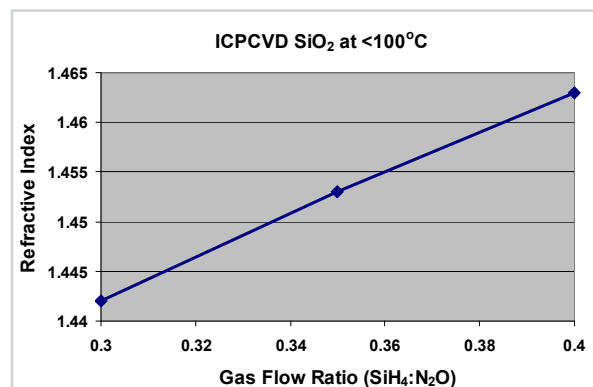


Figure 5: Variation of refractive index with SiH₄:N₂O gas ratio

Film Stress

In some applications such as MEMS the ability to control film stress is very important. Film stress is usually calculated by measuring the curvature change pre- and post-deposition of the film. This difference in curvature as a result of film deposition is used to calculate stress by way of Stoney’s equation, which relates the biaxial modulus of the substrate, thickness of the film and substrate, and the radius of curvatures of pre- and post-process.

In ICP-CVD silicon nitride and silicon oxide depositions the film stress can be controlled by changing various parameters. Process pressure has the biggest influence on the silicon nitride film stress and is shown in figure 6a below. By increasing the process pressure the film stress can be controlled from compressive to tensile. Figure 6a also shows that very low stress can be obtained by fine tuning the process pressure.

ICP-CVD silicon oxide films typically show compressive stress. The film stress can be adjusted by changing a combination of parameters including $\text{SiH}_4:\text{N}_2\text{O}$ ratio, temperature and RF power. Figures 6b and 6c below shows the effect of $\text{SiH}_4:\text{N}_2\text{O}$ gas ratio and temperature with film stress. Low compressive film stress can be obtained by increasing the $\text{SiH}_4:\text{N}_2\text{O}$ gas ratio and decreasing the deposition temperature.

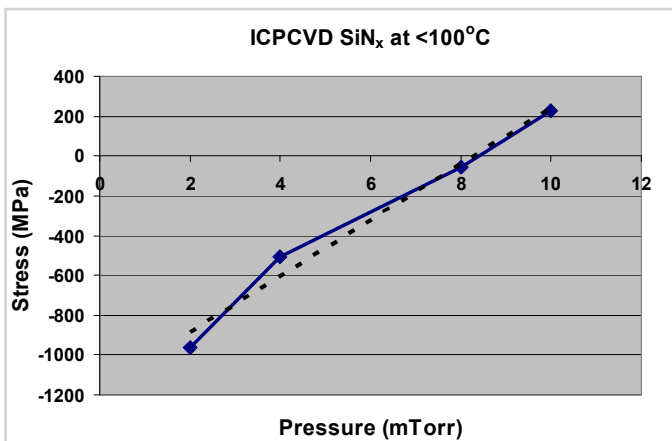


Figure 6a: Variation of Si_x film stress with process pressure

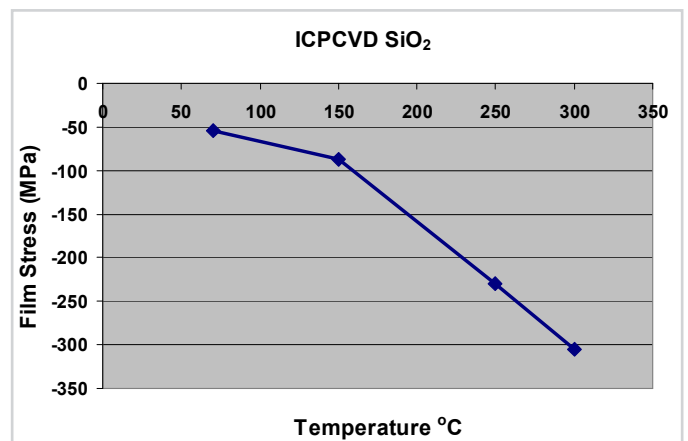


Figure 6b: Variation of SiO₂ film stress with temperature

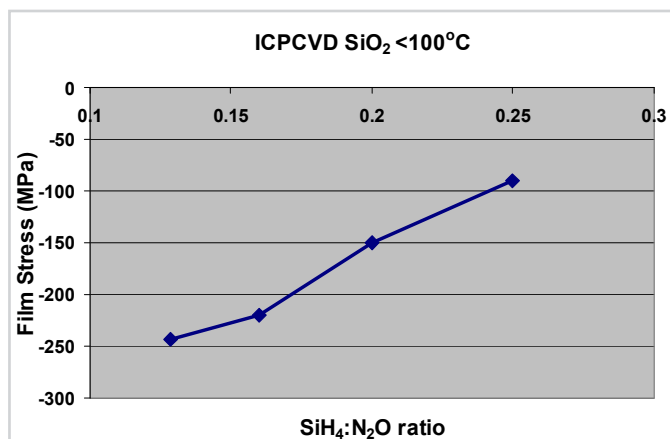


Figure 6c: Variation of SiO₂ film stress with SiH₄:N₂O gas ratio



Wet Etch rates

Quality of the film is most readily shown by wet etching, normally carried out with buffered oxide etchants (BOE) which are typically blends of 49% hydrofluoric acid (HF) and 40% ammonium fluoride (NH₄F) in various predetermined ratios. Typically BOE buffered oxide etchants are used to etch window openings in silicon dioxide layers. The primary application is the etching of thermal oxide layers in IC production. The etch rate of the film by aqueous NH₄F/HF solutions, with or without surfactant additives, depends on three primary factors: NH₄F range, etching temperature, and specific HF content. Standard BOE etchants (40% NH₄F/ 49% HF blends) contain over 30% NH₄F, a range where the HF content has primary influence on etch rate.

When testing wet etch rates of the film its usually good practice to measure the etching rate based on a thermal oxide layer as a reference. A low etching rate film usually indicates a high density film. Figures 7 and 8 shows wet etch rate data of SiN_x and SiO₂ deposited using both ICP-CVD and conventional PECVD. The data shows that films deposited at low temperature using ICP-CVD gives comparable film process performance with films deposited using high temperature conventional parallel plate PECVD at 300 °C.

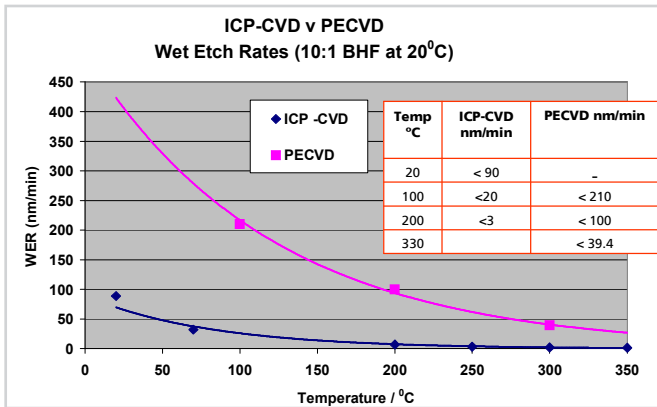


Figure 7: Variation of SiN_x wet Etch rate with electrode temperature

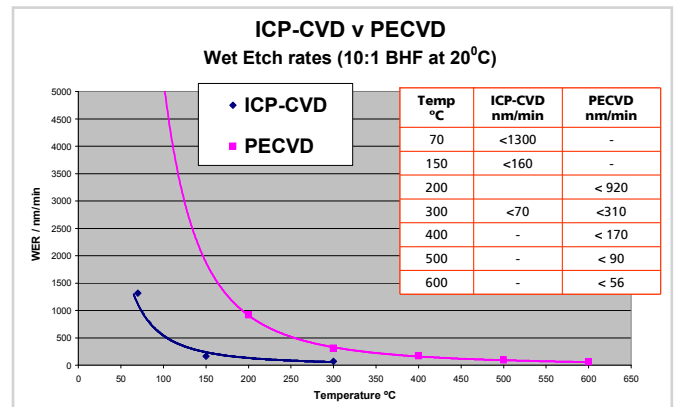


Figure 8: Variation of SiO₂ wet etch rate with electrode temperature

Breakdown Voltage

The breakdown voltage is usually measured by applying a ramped voltage across the dielectric film. The film is normally deposited on a conductive bottom layer (either a doped Si wafer, or a metal layer) together with a metal layer deposited on top of the deposited film. The metal layer is usually patterned either through a shadow mask or by lift-off to form small test pads (typically <<1x1mm). To contact to such small pads a wafer probe station is usually required. Al/Si metal layers are common but other metals could be used. It is important that the interfaces are flat and smooth, i.e. no hillocks or bumps on the underlying metal, and no particles on the surface or in the film, otherwise the breakdown voltage will be significantly reduced (the metal deposition process may need some optimisation if the customer does not have this set-up as a standard test already). This is one reason for having as small a test pad diameter since it is possible to minimise the chances of having a particle within your measurement area. The voltage is then ramped up until a high current peak is observed (i.e. breakdown of the film). The voltage required depends on the film thickness (e.g. 6MV/cm = 120Volts across a 2000Å thick film).



In ICP-CVD film depositions the electrical characteristics of SiN_x deposited at low temperatures ($\sim\text{RT}$) have shown breakdown electrical fields of more than $3 \times 10^6 \text{ Vcm}^{-1}$ with low leakage currents [1,2]. Table 2 below shows the effect of temperature on the breakdown voltage of ICP-CVD SiN_x deposited films.

In addition ICP-CVD SiO_2 also shows high breakdown voltage when deposited at low temperatures. Figure 9 shows the breakdown electrical fields of $>8\text{MV/cm}$ when the SiO_2 film was deposited at 150°C . In comparison a typical SiO_2 film deposited by PECVD at 300°C results in an electrical breakdown electrical fields in the range of $>5\text{-}6\text{MV/cm}$.

Temperature $^\circ\text{C}$	Breakdown Voltage ICP-CVD MV/cm	Breakdown Voltage PECVD MV/cm
20	> 3	-
150	> 7	> 3
200	-	> 4
300	-	> 5

Table 2: ICP-CVD SiN_x typical breakdown voltage values

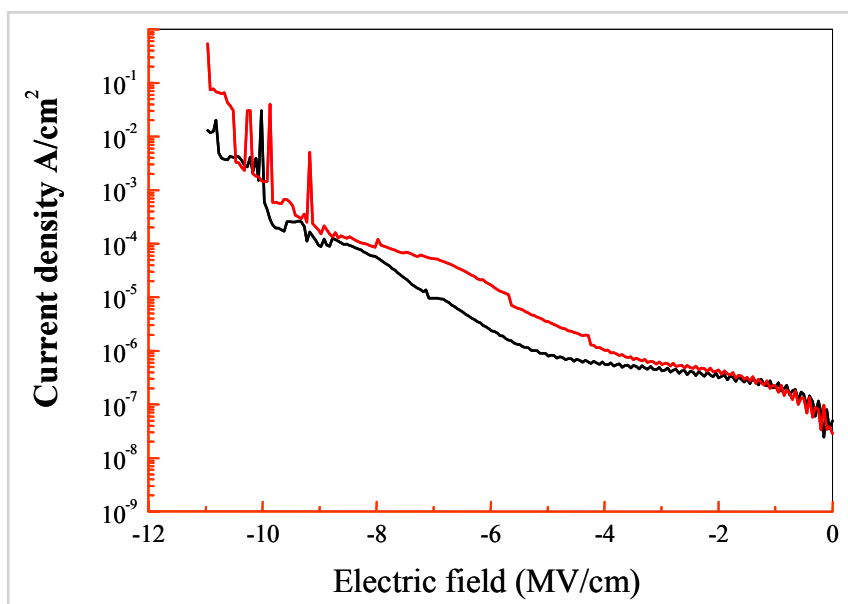


Figure 9: Variation of current density with electric field for ICP-CVD SiO_2 film deposited 120°C . The results show breakdown voltage $\sim>8\text{MV/cm}$.

Step Coverage

The step coverage is the ratio of film thickness along the walls of a step to the thickness of film at the bottom of the step. This is referred to S/T and/or S/B in the figure (*) below. For conformal coverage the ratio of S/T and/or S/B is 1. Typically good step coverage is achieved by using high temperatures ($>300^\circ\text{C}$) however it is possible to achieve excellent step coverage at low temperature using ICP-CVD. Figure (*) below shows ICP-CVD SiN_x film coverage when deposited at 20°C . In addition the step coverage also depends on the step height and width.

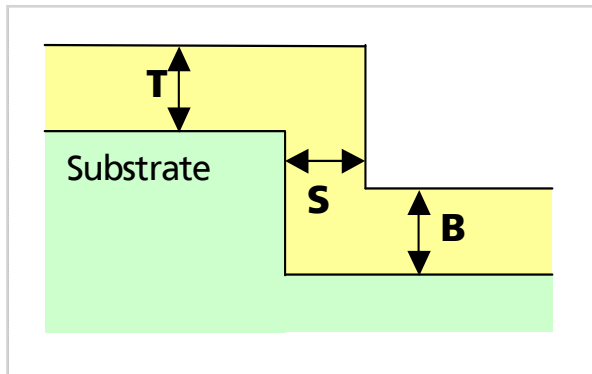


Figure 10a: (Above) Definition of step coverage

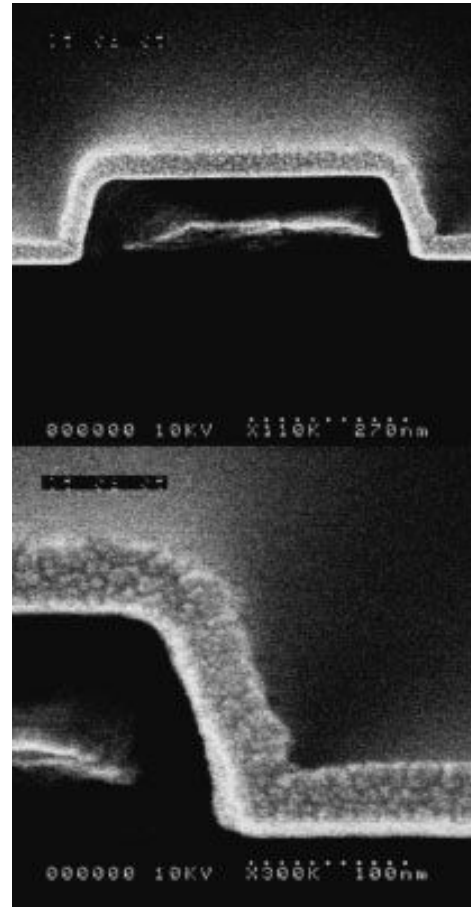


Figure 10b: (Right) SEM images of cross section of 50 nm ICP-CVD SiN deposited at 22°C on 150 nm metal with good step coverage.

Courtesy of University of Glasgow [2]

Oxford Instruments Plasma Technology's New Process Improvements

Film Thickness Uniformity

Process improvements have also been made in which improved film thickness uniformity has been achieved based on our new patented hardware design [3]. The new hardware design also allows the user the ability to deposit layers over larger areas with excellent film thickness uniformity. The patented hardware design is based on a new style showerhead design which we call a transmission plate. The transmission plate is then placed in the chamber and sits between the high density plasma source and the substrate.

The transmission plate has been optimized by adjusting the hole sizes and distribution in order to achieve maximum film thickness improvement. The transmission plate is made of the aluminium alloy 6082 with sufficient thickness to maintain the plate close to the chamber temperature by lateral conduction, even when running with high ICP powers. It was found that in order to achieve "best" film thickness uniformity for silicon nitride and silicon oxide depositions two different variants of the plates were required.

Figures 11 and 12 (below) show two different transmission plates for an ICP180 source.

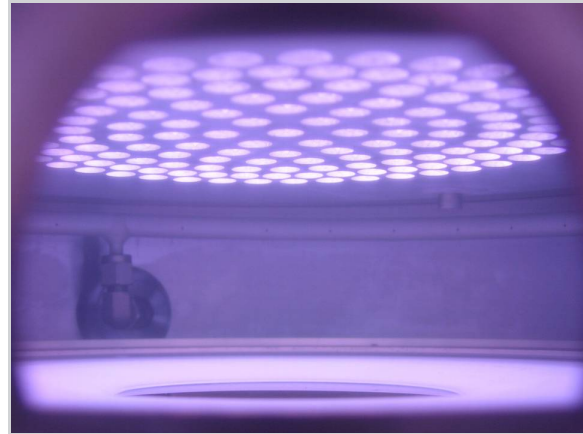


Figure 11: Image of the silane gas ring and gas transmission plate inside the process chamber during a plasma process

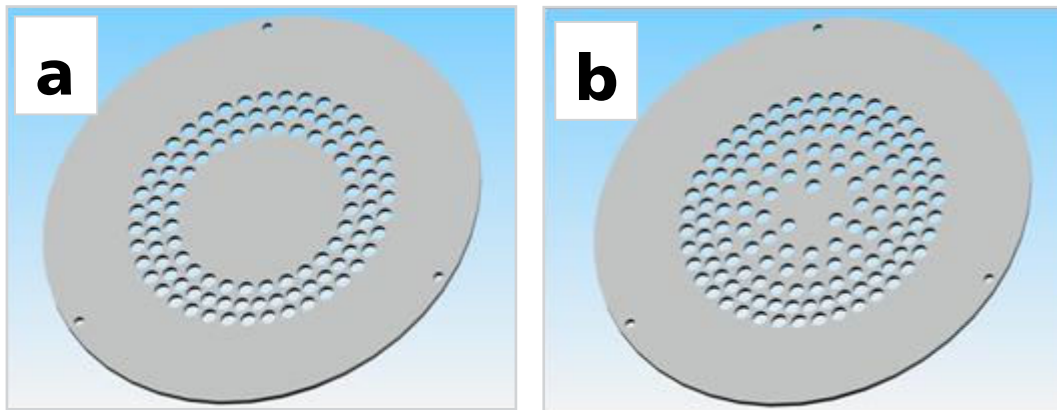


Figure 12: Two gas transmission plates.
(a) Transmission plate 1 is optimised to deposit SiO_2 . (b) Transmission plate 2 is optimised to deposit SiN_x .

Figure 13 shows a larger transmission plate which is required for the ICP380 source in order to deposit ICP-CVD films with substrates up to 300mm with excellent film thickness uniformity.



Figure 13: Transmission plate used with the ICP380 source

Figure 14 and 15 shows an example of SiN_x film thickness distribution over 100 mm and 200mm silicon wafer, using an ICP180 and an ICP380 source respectively. Oxford Instruments' ICP-CVD systems now offer these improved process improvements, and users will also be able to easily upgrade their existing ICP-CVD system in order to able to achieve even better film performance.

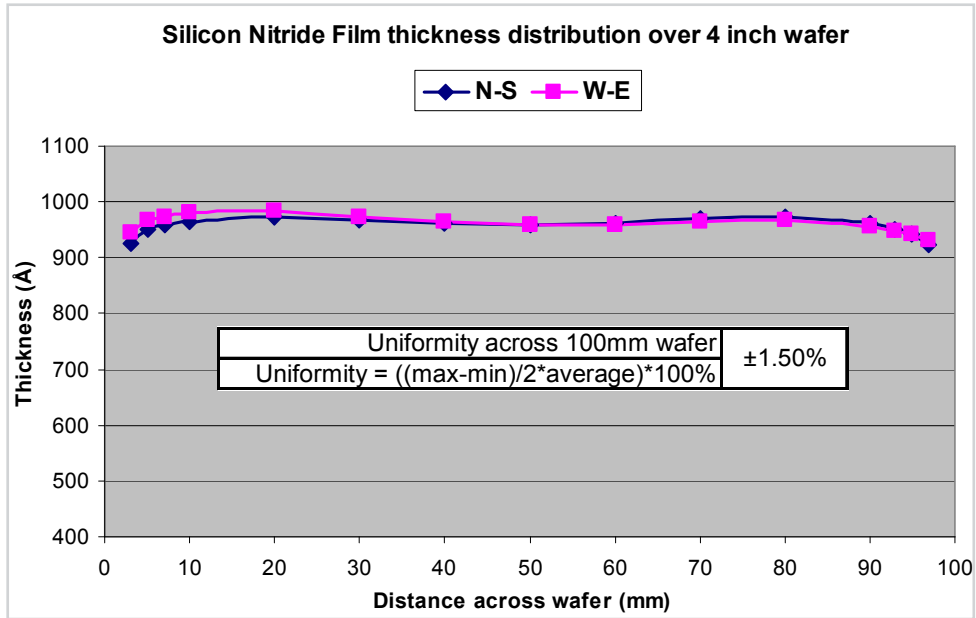


Figure 14: ICP-CVD SiN_x film thickness uniformity over 100mm using a System100 with an ICP180 source

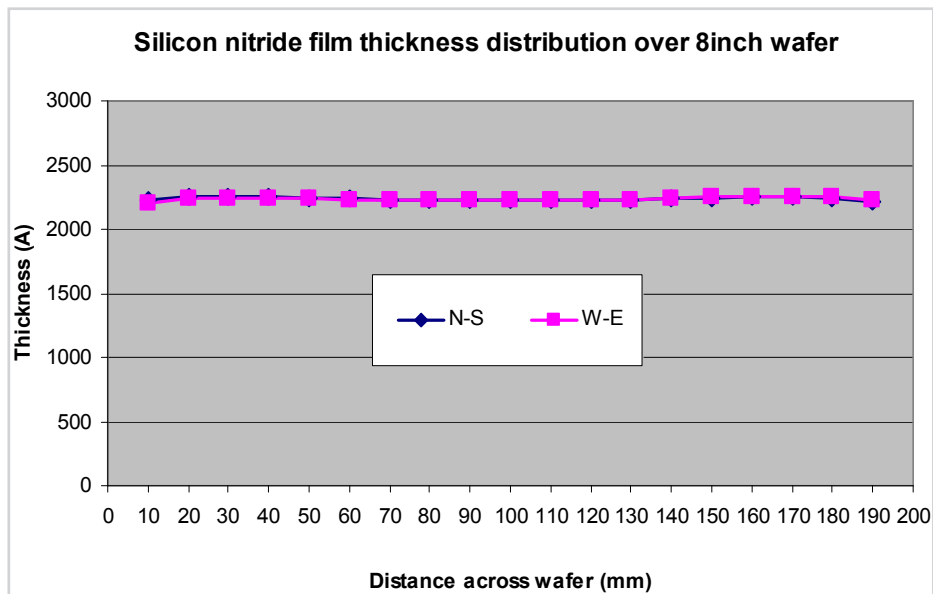


Figure 15: ICP-CVD SiN_x film thickness uniformity over 200mm using a System100 with an ICP380 source



Typical film thickness uniformity performance for low temperature depositions also depends on the ICP source used. Table 3 shows the different film thickness uniformity depending on the ICP source.

ICP Source	Wafer Size			
	50mm	100mm	150mm	200mm
ICP65	<±6%	-	-	-
ICP180	<±2%	<±3%	<±5%	-
ICP380	<±1%	<±2%	<±3%	<±5%

Table 3: Typical ICP-CVD film thickness uniformities

ICP-CVD for production

High deposition Rate depositions

Deposited films such as Silicon nitride and silicon oxide are used in HBLEDs to passivate the final devices. Current methods include batch PECVD processing which has a typical load of up to 8 x 4" substrates (and a much larger load of 2" substrates) with a growth rate of 14-15 nm/min. Considerable amount of interest recently have been directed towards single wafer LED processing which requires higher deposition rates to maintain throughput requirements. It is also known that the deposition temperature must also be kept as low as possible. These requirements restricts the ability of conventional PECVD which require high temperatures and low deposition rates in order to allow high quality material to be deposited, probably through allowing sufficient time for excess hydrogen to outgas from the growing film.

We have already discussed that high density films can be deposited at low temperatures (<150°C) using the ICP-CVD technique but with typical deposition rates of 8nm/min. However recent development work at OIPT has achieved much higher deposition rates of > 140nm/min at the same low temperatures, whilst maintaining good film quality, film thickness uniformity and film stress control. These recent advances have shown the capability of ICP-CVD in achieving high quality films at low temperatures with high throughput. The higher deposition rate processes were achieved by increasing the ICP power and gas flow mixture as shown in figure 16 below. The gas flow ratio for SiN and SiO₂ deposition were then adjusted in order to tune the refractive index (figure 17).

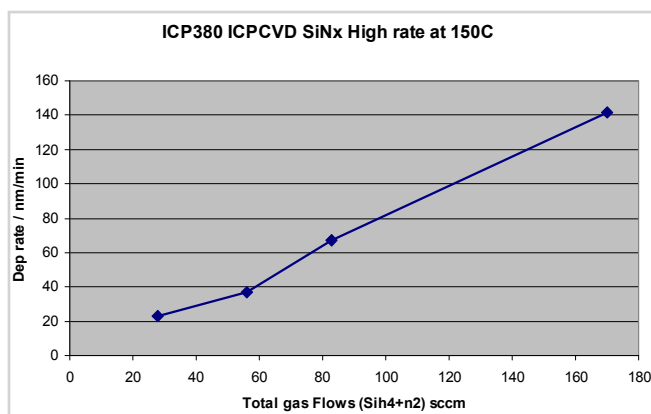


Figure 16: Variation of deposition rate with total gas flows for ICP-CVD SiN_x deposited at 150°C

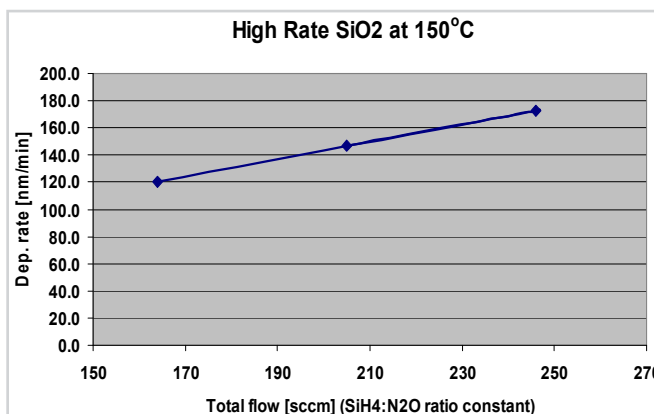


Figure 17: Variation of deposition rate versus total gas flows for ICP-CVD SiO₂ deposited at 150°C

Process Repeatability

One of the most important factors of a deposition system is the ability to deposit the same film over and over again. The repeatability and stability of the ICP-CVD process in which tests have been carried out by depositing high deposition rate SiO₂ (>140nm/min) at low temperatures (<150°C) on 75 x 100mm wafers. Results are shown in figure 18, 19, and 20 below.

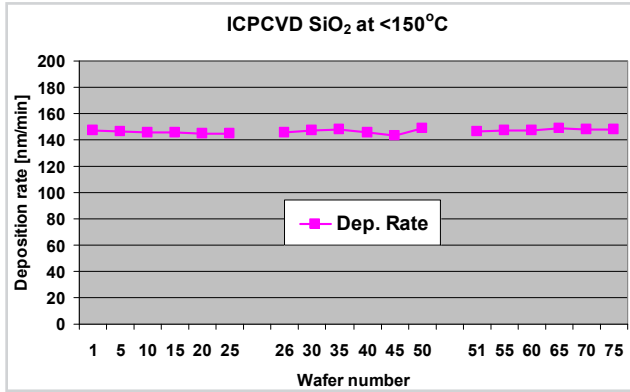


Figure 18: Wafer to wafer deposition rate repeatability of <+/-2% with film thickness uniformity of <+/-3% over 100mm wafer

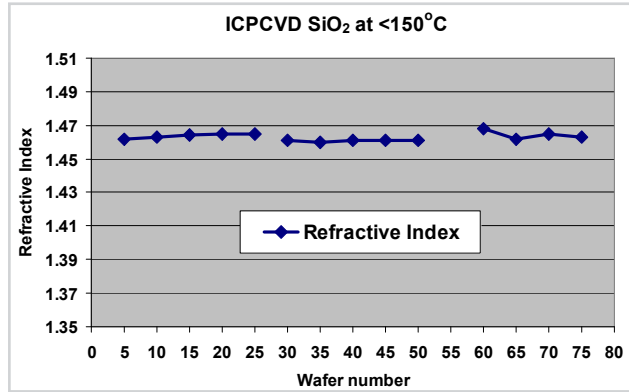


Figure 19: Wafer to wafer refractive index repeatability of <+/-0.3%

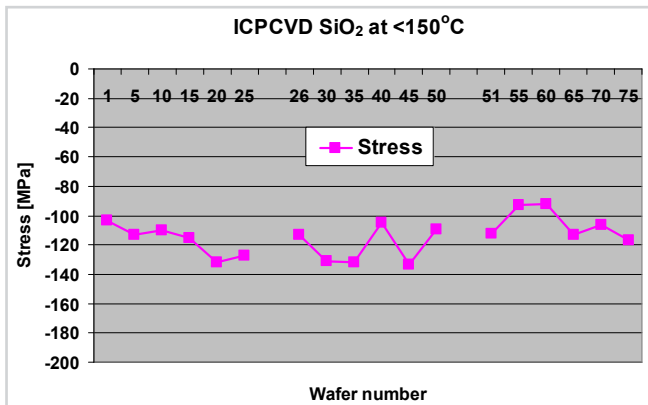


Figure 20: ICPCVD SiO₂ film stress repeatability over 75 wafers

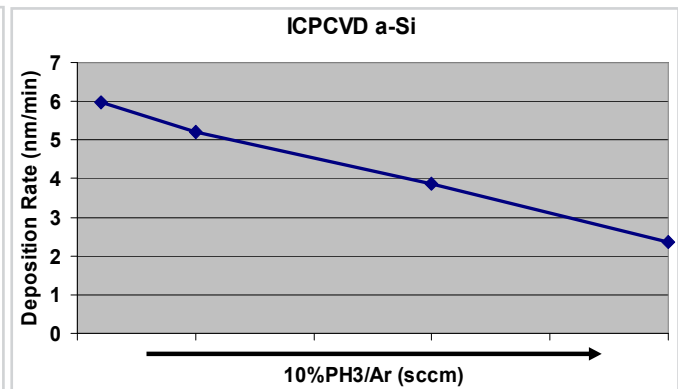


Figure 21: Effect of phosphorous gas flow on ICP-CVD a-Si deposition rate

ICP-CVD amorphous silicon and ICP-CVD silicon carbide

In addition to SiO₂, SiO_xN_y and SiN_x layers ICP-CVD can also be used to deposit other materials such as amorphous silicon (undoped and doped) and silicon carbide.

Amorphous silicon is usually deposited using pure silane with small flows of argon in order to help strike the plasma. Additional hydrogen is also used in order to improve the film quality. Dopants can be added in the form of phosphorus and boron in order to change the conductivity of the layer which is particular important in photovoltaics applications. Figure 21 below the effect of Phosphorous flow on deposition rate for ICP-CVD amorphous si layers.

ICP-CVD can also be used to deposit silicon carbide. Silane is normally mixed with methane and argon is also used to help with plasma striking. The refractive index of the SiC can be tuned by adjusting the gas flow ratio of silane to methane. Figure 22 and 23 shows the relationship between refractive index, film stress and methane/silane gas flow ratio.



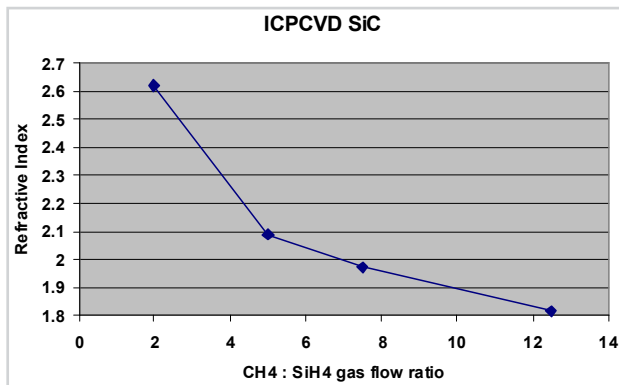


Figure 22: Variation of refractive index with methane/silane gas flow ratio

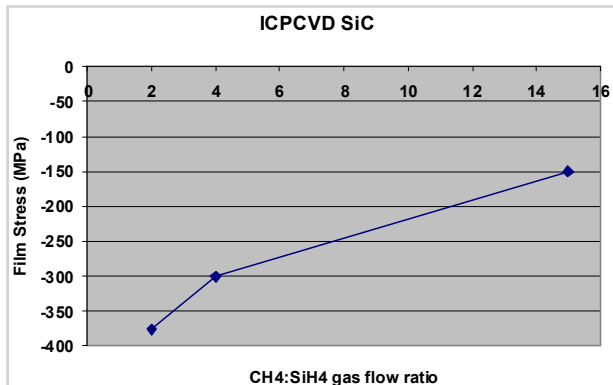


Figure 23: Variation of film stress with methane / silane gas flow ratio

ICP-CVD Plasma cleaning

Chamber Plasma cleaning

In ICP-CVD processing, a significant proportion of the tool time is devoted to plasma cleaning using etching gases to clean the process chamber. There are a number of clean gases available such as CF₄, C₃F₈, C₂F₆ and NF₃. However in our ICP chambers we nominally use SF₆ due to ability to achieve higher etching rates, cleaner by products and experienced etching processes which we have modified in order to successfully clean inside the chamber. Alternative gases which we have also used are CF₄ and C₃F₈.

The clean gases whether its SF₆ or CF₄ is usually used with either O₂ or N₂O in order to reduce the by products formed after the clean. The clean consists of using the ICP power and also power to the electrode. This is used to promote the fluorine in order to achieve faster etching rates. A wafer is also suggested to be placed on the table in order to protect the surface i.e. reduce over cleaning in this area. The plasma cleaning time and the cleaning intervals depends on the nature of the deposition. For example if a high stress film is deposited in the chamber then the maximum deposition before cleaning is required is reduced due to the potential of the film flaking from the chamber walls onto the sample. Typical thickness and cleaning guidelines are shown below.

- Cleaning should be carried out after >5microns of film deposition.
- Cleaning time is dependent on type and thickness of film deposited.
- Typical cleaning time is 2hours for 6-8 microns of film deposition.

Following a plasma chamber clean it is important to run a pump purge recipe in order to minimise particulates. A typical sequence is shown below:-

Repeat 30 times/1min pump/1min N₂ purge, 100sccm, 50mT/Loop

Conditioning of the chamber is an important step in order to achieve a repeatable process. We have observed that ~0.5microns of deposition is required for conditioning. Figure 24 shows how the deposition rate and refractive of the process stabilises after a chamber plasma clean and chamber conditioning.

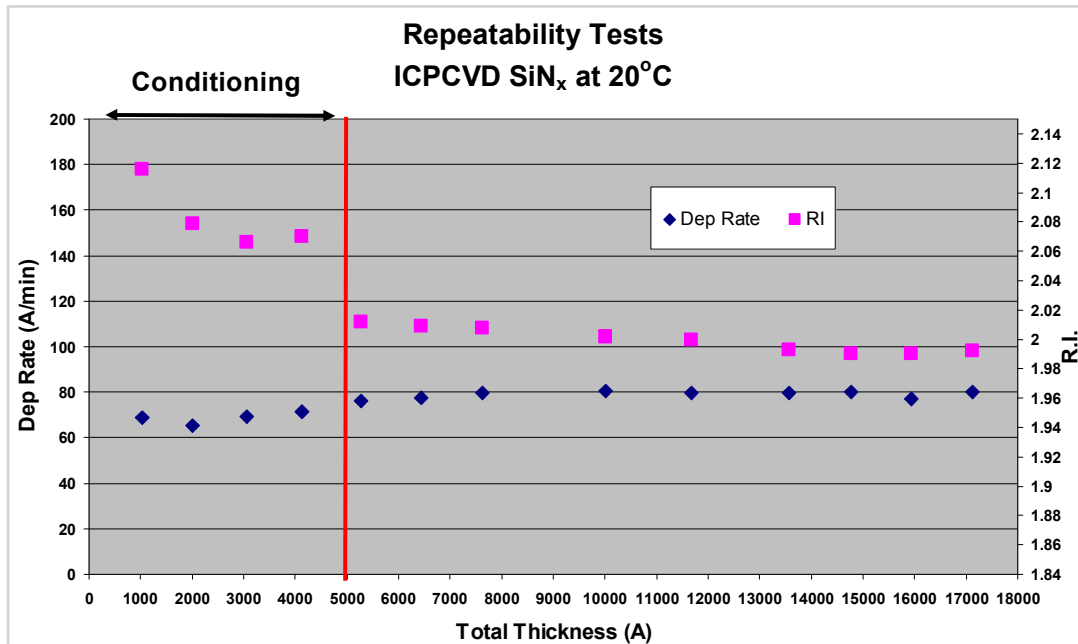


Figure 24: Effect of chamber conditioning on process repeatability

Surface precleaning

A plasma pre-treatment process can be applied to a particular surface in order to avoid delamination of the deposited films especially when the film comes under some thermal or mechanical stress. Good adhesion of the deposited films onto the underlying material depends on the type of surface and also the type of residues on the surface. Oxygen based plasma pre-clean has the greater effect in removing organic residues whereas a hydrogen based plasma pre-clean has the greater effect removing inorganic residues.

If a substrate material other than Silicon is used such as Gallium Arsenide or Gallium nitride a plasma pre treatment process is essential to achieve good film properties. For example, adhesion and quality of the deposited film can be improved by applying a hydrogen based pre clean process prior film deposition. This has been carried out by using an ammonia/nitrogen plasma pre clean where the ammonia dissociates into nitrogen and hydrogen and the resulting hydrogen attacks the underlying surface giving a hydrogenated surface which provides a good interlayer between film and substrate. The subsequent deposited film then shows good film properties such as good adhesion, low pinholes and good electrical characteristics.

Summary

In this paper we have shown that ICP-CVD can be used to deposit various materials including SiO₂, SiN_x, a-Si and SiC. By using the ICP-CVD technique high quality films are deposited with high density plasma, low deposition pressures and temperatures which results in minimizing film contamination, promoting film stoichiometry, reducing radiation damage by direct ion-surface interaction, and eliminating device degradation at high temperatures.

References

- [1] K. Elgaid, H. P. Zhou, C. D. W. Wilkinson and I. G. Thayne: Microelectronic Engineering 73–74 (2004) pp. 452–455.
- [2] H. P. Zhou, K. Elgaid, C. D. W. Wilkinson and I. G. Thayne: Japanese Journal of Applied Physics Vol. 45, No. 10B (2006) pp. 8388–8392
- [3] EP1889946A2 'Surface processing apparatus' O Thomas, AJV Griffiths, MJ Cooke (2007)