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Dry Etching of InP based Materials using a high density ICP plasma system

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1 Introduction

Dry etching is now widely used in the fabrication of optoelectronic and electronic devices involving III-V materials, due to the need for careful control of the critical dimensions of components. Fast etch rates, repeatability, uniformity, clean chemistries, vertical profile, low device damage are some of the most desirable aspects of the etching process. Inductively coupled plasma (ICP) etching is ideally suited to these requirements, since it provides a high ion density; hence fast etch rates, while allowing separate control of ion density and ion energy, giving a low damage capability.

Oxford Instruments Plasma Technology (OIPT) has developed a wide range of ICP etch processes for III-V semiconductors to meet these demands.

In this article, we will focus on etching process for InP and related materials, discuss various etching chemistries and system requirements for different applications and provide an update of the latest new process developing results.

2 The ICP tool

The system used for these processes is the Oxford Instruments Plasma Technology **Plasmalab** System 100 ICP etcher (OIPT CS1 hardware). A schematic of the etch chamber is given in Figure 1 and the full system is shown in Figure 2.

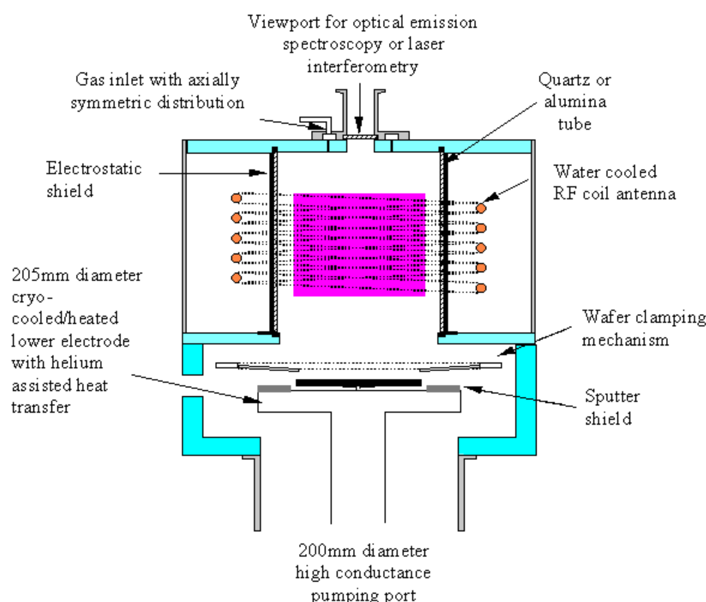

Figure 1 Schematic of the Plasmalab System100 ICP180 tool

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Figure 2 ***Plasmalab System 100 ICP180***

RF power (13.56MHz) is applied to both the ICP source (up to 3000Watts) and substrate electrode (up to 600Watts) to generate the etch plasma. An electrostatic shield around the ICP tube is used to ensure that the ICP power is purely inductively coupled (i.e. 'true-ICP'), hence eliminating sputtering of tube material and minimising unnecessary high-energy ion damage to devices. Ion energy at the substrate is monitored by measurement of the DC bias generated on the lower electrode, and is controlled mainly by the RF power supplied to this electrode.

Wafers are loaded into the chamber via a loadlock to maintain good stability of chamber vacuum and hence repeatability of etching results.

The wafers being etched are either mechanically or electrostatically clamped to the temperature-controlled lower electrode. Helium pressure is applied to the back of the wafers to provide good thermal conductance between the chuck and the wafer. Where necessary, smaller samples are attached on 4" Silicon carrier wafers with thermally conductive glue.

The Plasmalab System100 ICP has control of substrate temperature to accuracy of ±1°C over a temperature range of -5°C to +400°C, through the use of electrical heater elements and a coolant circulating circuit. This can be extended to –150ºC to +400ºC with the addition of a supply of liquid nitrogen. Substrate temperature has a marked effect on the etch result, as it controls the volatility of the etch species and hence influences the chemical component of the process, affecting not only etch rate, selectivity and profile, but also surface roughness. The system can be operated over a pressure range from 1mT to 100mT allowing accurate control process chamber pressure.

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3 InP based Material Etching

3.1 High Rate Etching of Waveguide and Mirror Facet

For the high rate etching of mirror facet and waveguide, the key requirements are fast etch rates to depths of up to 10µm and 5µm respectively, controllable etch depth, highly anisotropic profile, no notching at buried layers of InGaAsP (or similar), and smooth sidewalls and etched surface.

$CH_4/H_2/Cl_2$ chemistry is the most popular process for this kind of application. If the temperature of the wafer is allowed to increase to near 200ºC then the etch rate of the commonly used CH_4/H_2 process increases, however, profile control becomes difficult due to increased undercutting. Addition of Cl_2 to this mixture allows highly anisotropic etch profiles, due to the low volatility of $InCl_x$. This therefore allows accurate profile control through adjustment of CH_4/Cl_2 ratio. Etch rates of >1.5µm/min and selectivities of >15:1 to SiO_2 or SiN_x masks can be achieved. Figure 3 shows a 10µm deep mirror facet etched using this chemistry.

This chemistry has the advantage that it etches a wide range of materials, i.e. those containing In, P, Ga, As, Al, Sb etc, with low selectivity (~0.5-1:1) between each other, hence etched profiles have no notching at interfaces between materials. It also produces less polymer contamination than the CH_4/H_2 chemistry due to the lower CH_4 content of this process and much faster etch rate. There is no additional wafer heating required, as the InP based wafer is heated solely by the high density plasma itself. With accurate control of the plasma parameters, process repeatability is better than ±3%, and no wafer clamping is required.

This technique enables batch processing for high throughput production applications, e.g. 4x2" wafer loaded per run, since the wafers can simply rest on a carrier plate and do not need to be individually clamped and helium cooled. Another variant of this process is the $CH_4/Ar/Cl_2$ chemistry which has also been shown to produce excellent etch results using this etch chamber.

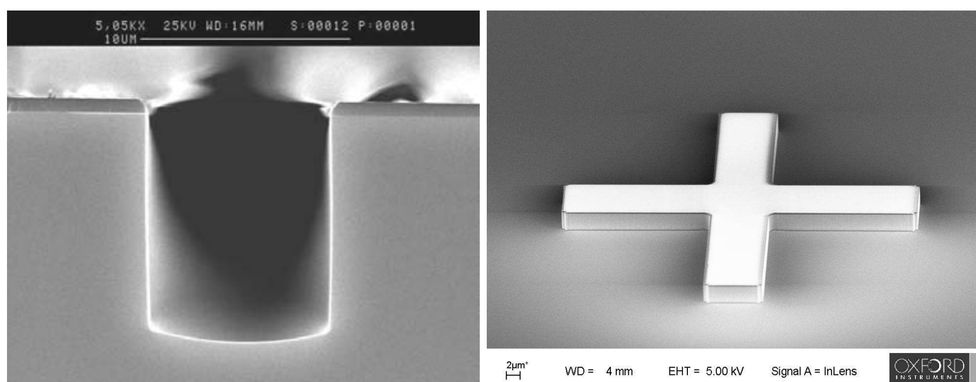

Figure 3: ***InP based material etched using $CH_4/H_2/Cl_2$ process. Etch rates of >1.5µm/min and selectivity of >15: are achieved.***

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	Etch rate (nm/min)	Selectivity to SiO_2	Etched profile	Etched surface and sidewall	Uniformity
Single 2'wafer	1500	15:1	90°±1*	smooth	<±2.5%
Single 4'wafer	500	8	90°±1*	smooth	<±4.0%
Batch 4x2'wafers	500	8	90°±1*	smooth	<±4.0%

Oxide mask profile is required to be better than 80 degree

Table 1*: $CH_4/H_2/Cl_2$ process performance summary*

However, often the demands of production dictate that the chamber must stay as clean as possible, ideally with no polymer deposition, even at the expense of the etch anisotropy and sidewall smoothness if necessary. This requires that the process does not contain CH_4. A common approach is to use a Cl_2 based etch chemistry with a heated electrode (150°C in order to effectively remove the $InCl_x$ etch product from the wafer surface).

Accurate wafer temperature control is recommended for this process. If the sample gets too hot the $InCl_x$ 'evaporates' from the surface easily and hence produces undercutting. On the other hand, at too low a temperature $InCl_x$ is non-volatile resulting in slow etch rates, low selectivity and surface roughness. Often N_2 is added to increase the physical component of the etching and to passivate the surface, hence reducing surface roughness and improving profile control. Etch rates of >1 μm/min and selectivity to SiO_2 of >10:1 have been achieved using this process. Figure 4 shows a typical 5μm deep etch result. This is a H^+ free process which may give less damage to device, since H^+ often forms a passivation layer at the etched surface that may affect device performance.

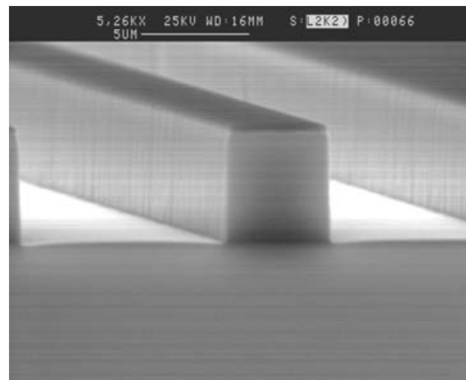

Figure 4 ***Cl_2/N_2 etched waveguide***

The $CH_4/H_2/Cl_2$ and Cl_2/N_2 processes listed above can also be used to create device mesas, with either vertical or sloped profiles achieved by suitably adjust process parameters.

An alternative technique which allows processing at lower temperatures of ~100-150°C involves the use of HBr chemistry, since the etch product of $InBr_x$ becomes volatile at a lower temperature than $InCl_x$. Figure 5 shows a typical 5μm deep etch result at an etch rate of 0.8μm/min and a selectivity of >10:1 to SiO_2. Again, good temperature control is recommended due to the sensitivity of etch results to wafer temperature.

The HBr process can also etch InP with photoresist (PR) as a mask as shown in figure 6 since it requires lower temperature compare to Cl_2 chemistry. Typically an etch rate of >1μm/min and a selectivity of 14:1 are achieved. This process required hard baking of photoresist mask before etching in order to reduce photoresist burning. Advantages of this process include potential elimination of the use of hard masks and significantly reduce process complexity and cost.

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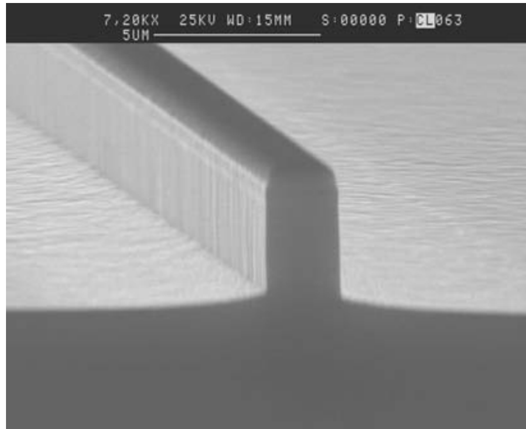

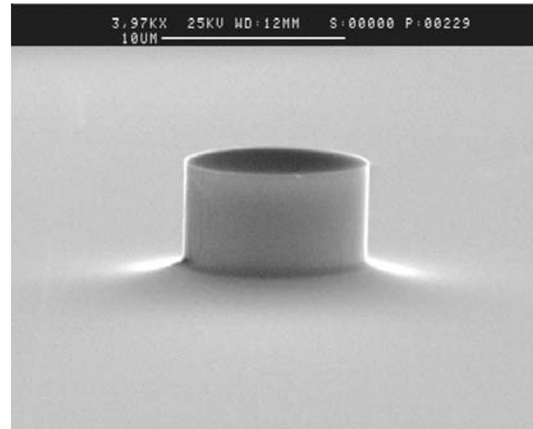

Figure 5 ***HBr waveguide etch*** Figure 6 ***InP etches using photoresists as a mask***

A Cl_2/H_2 process has been developed recently. In this process, the lower electrode is set at room temperature. The wafer is placed on top of a carrier wafer without additional thermal contact. No wafer clamping is required. Therefore it is a simple process. The etch mechanism is similar to the $CH_4/H_2/Cl_2$ process - the wafer is heated by the plasma itself. The advantage of this process is the absence of CH_4, therefore no polymer depositing in the chamber. It is a clean and also environmental friendly process. In this process, the gas ratio of Cl_2/H_2 is very important. High gas ratio leads to high etch rate but also gives an undercut etching profile. Figure 7 shows the results of Cl_2/H_2 etch in ICP mode. The etch rate is 850nm/min with selectivity to nitride mask of > 10:1.

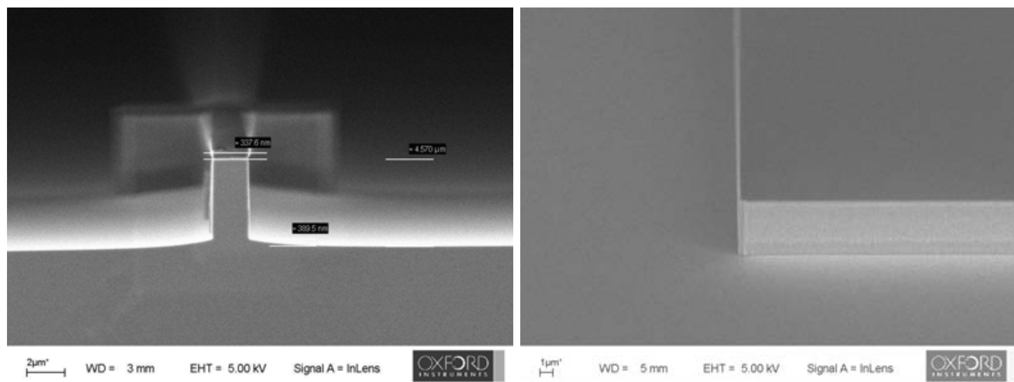

Figure 7 ***InP/InGaAs sample etched using Cl_2/H_2 process at room temperature.***

3.2 InP Grating Etching or shallow etching

Although InP etching process can be replaced by faster, cleaner etch chemistries in ICP mode for the majority of applications, however, the CH_4/H_2 process is still widely used for InP DFB(distributed feedback lasers) grating etching, due to the requirements of shallow, accurately controlled etch depth (typically <200nm). Also the frequent use of photoresist masks, often delicate e-beam resists, for grating definition requires room temperature etching. In an ICP tool this process is typically performed with no ICP power, i.e. only lower electrode power is applied, enabling a slow 'RIE mode' of etching. Figure 8 shows the result of a RIE mode grating etch in an ICP tool to a depth of 100nm at an etch rate of 20nm/min.

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Figure 8 ***CH_4/H_2 grating etch***

CH_4/H_2 process in RIE mode is a popular for shallow InP etch (etched depth less than 1000nm). Since it is a room temperature process, photoresist can be used as mask. However, CH_4/H_2 forms a large amount of polymer in the chamber and also deposit at etched top surface and sidewall. Often a short O2 clean step is added into the process following the etching in order to remove the residual polymer. Figure 9 shows the result of a RIE mode shallow InP etch to a depth of less than1000nm at an etch rate of 20~40nm/min.

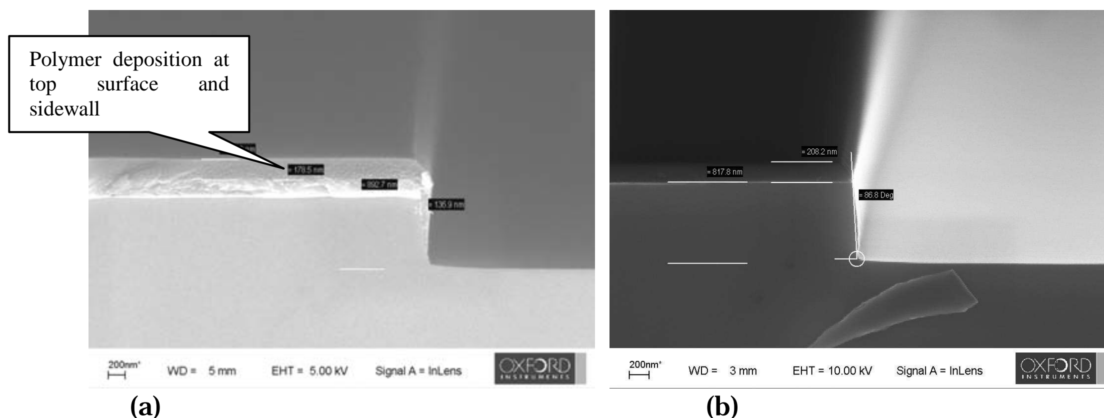

Figure 9 ***shallow InP etch using CH_4/H_2 process, (a) single step process showing some polymer deposit on the etched top surface and sidewall. (b) Two step process, no more polymer residual on etched surface.***

CH_4/H_2 chemistry is also commonly used for InGaAs/InAlAs selective etching due to the requirements of shallow etch depth, and selectivity between InGaAs and InAlAs.

$CH_4/H_2/Cl_2$, Cl_2/N_2, and HBr in ICP mode processes can also be used for shallow etch. If the sample is pre-heated to above 150 degree by the lower electrode, it has been shown to be possible to reduce the etch rate from >1µm/min to 0.2µm/min[4] by choosing low ICP power. A typical etched profile is shown in Figure 10.

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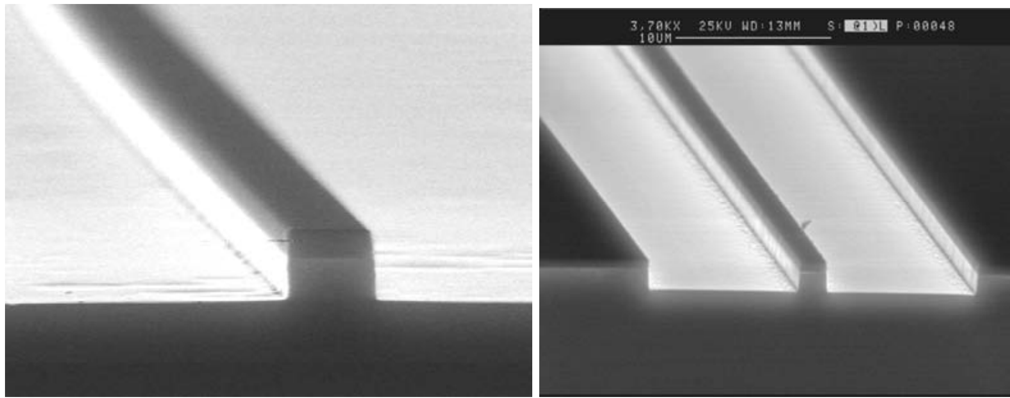

Figure 10 ***Controllable etch rate for shallow etching***

3.3 InP photonic crystal (PhC) etching

Etching of InP photonic crystal waveguide structure is very challenging, since it requires high aspect ratio with feature sizes under half a micron. The most popular structure is two dimension hole type with hole size less than 500nm.

All InP etched process motioned above can be employed to etch PhC. P Strasser from ZTH Zurich developed an etching process using ICP180. The conclusion from his work is that $Cl_2/N_2/Ar$ is the best chemistries for PhC etch. This is a polymer free process, and also provides a square foot as shown in Figure 11. The wafer temperature is set at above 200degree, Cl2 is a etch gas, Ar is used as a dilute gas and N2 gives passivation at the sidewall. An aspect ratio of >15:1 was achieved. Figure 10 shows an etched depth of 2.9µm and etch rate of 1.75micron/min achieved for 190nm diameter hole size, which gives aspect ratio ~16:1. The small sample pieces have to be glued on to the carrier plate and backside Helium cooling is required.

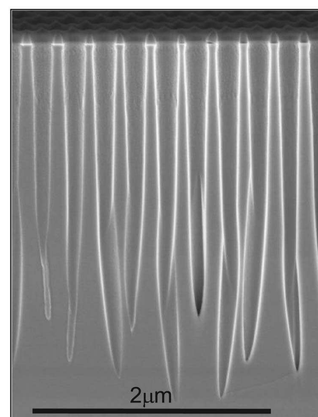

Figure 11 ***PhC etched in InP. The holes have a diameter of 180nm and etched depth is 2.9microm. (With kind permission of P Strasser, etc. Communication Photonics Group ETH Zurich)***

3.4 InP Via Hole Etching

The requirements for InP via hole etching are somewhat different, i.e. fastest possible etch rates to depths of up to 150µm, near vertical or slightly sloped etch profile, resist masked (ideally), flat smooth base, but no concern about sidewall smoothness. These requirements can be met through the use of an HBr/BCl_3 based etch process at moderate to high temperatures (120-180ºC). The photoresist mask must be thoroughly hard-baked to a high temperature (>150ºC) to ensure that it survives the etch process without reticulation. Figure 12 shows a 100µm deep via hole etched using this technique. Etch rate was >2.75µm/min and selectivity to photoresist >15:1.

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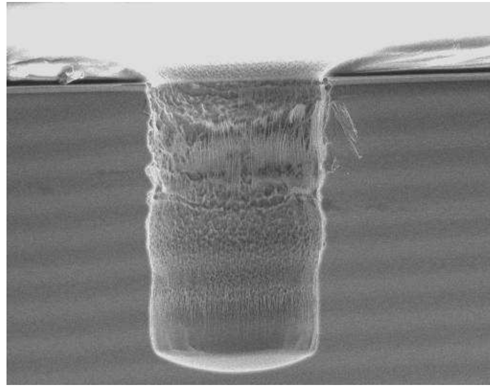

Figure 12 ***HBr/BCl$_2$ process for InP Via hole etch***

3.5 InP/InGaP/AlInP red LED and solar cell etching

InP/InGaP/AlInP based material combinations are widely used for making red LED's or Solar cell's. Requirements for both red LED and solar cell products are high yields and low cost. Therefore a batch process is essential, also photoresist is chosen for simplified process and low cost.
$BCl_3/Cl_2/Ar/CH_4$ is used. The optimised process is unclamped. Table temperature is kept at 20~30degree, give a etch rate of 450nm/min with selectivity to photoresist mask of 3:1 and etched profile as shown in Figure 13.

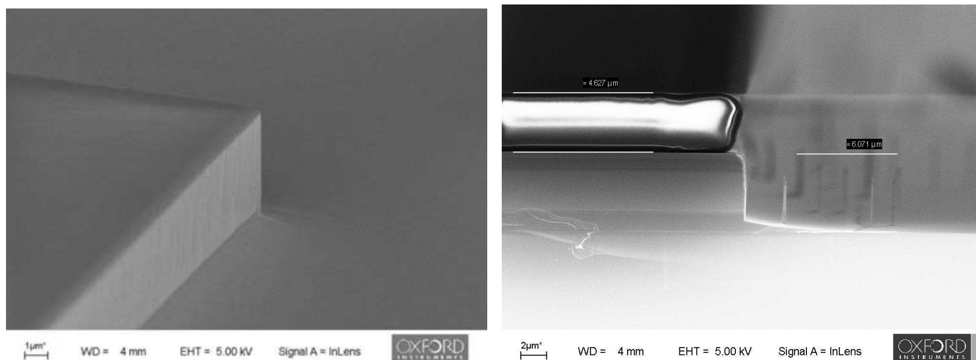

Figure 13 ***InP based Solar cell etched using $BCl_3/Cl_2/Ar/CH_4$, Photoresist was used as a etch mask***

3.6 InP MicroLens Etching

Microlenses which are commonly used for advanced photonic applications are formed in photoresist using one of two techniques. The simplest technique involves forming squat cylinders of resist using conventional lithography. The substrate is then heated above the glass reflow temperature of the photoresist (i.e. 130-150ºC), allowing it to reflow. This will create a spherical surface, with the radius that may be calculated from the volume of resist and the area of contact with the substrate. The lens profile is then transferred into the substrate material by ICP dry etching, often with 1:1 selectivity.

Figure 14 shows a SEM image of a microlens etched into InP to a depth of 20μm. This was created by resist reflow combined with ICP etching. In this case it is possible to adjust the selectivity between the InP and the photoresist either by changing the gas mixture used for the process or by adjusting the ICP power and/or DC bias between the plasma and the substrate. Increasing the selectivity (so the photoresist etches more slowly) will increase the curvature of the finished lens. As the gas mixture used for this process includes chlorine there is the likelihood of post-etch 'bubbles' forming on the etched surface when the

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wafer is removed from the tool, due to the hydrophilic nature of chlorine. OIPT has developed a proprietary technique that avoids this effect and provides a smooth etched surface.

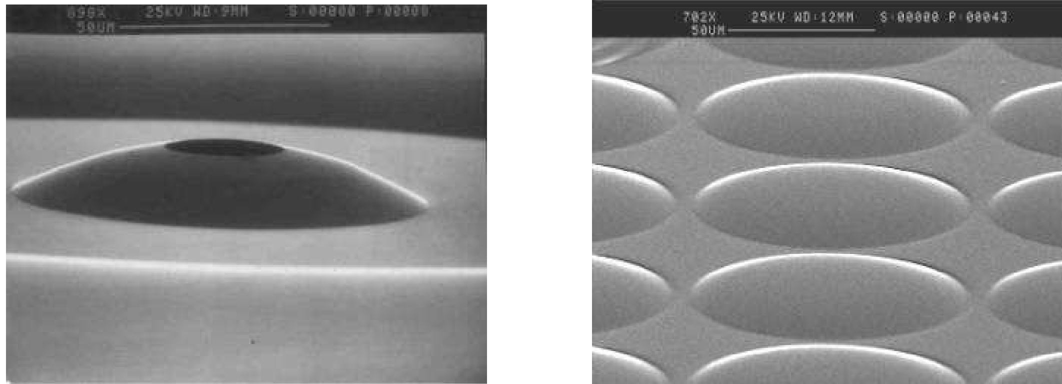

Figure 14 ***Microlens etched into InP (a small amount of photoresist is visible on the left SEM image, highlighting the etch procedure).***

5 Summary

InP based material etching is a vital technology for the fabrication of optoelectronic and electronic devices.

Oxford Instruments Plasma Technology's System100 ICP etcher (OIPT CS1 hardware) provides wide ranges of III-V material etching solutions. Highly vertical (or controlled slope) etched profile, smooth sidewall, with good selectivity to oxide, nitride or PR mask, and controllable etch rate can be achieved.

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