APPLICATION NOTE

# Ultra-high resolution EBSD analysis of fine copper interconnect lines

## QUESTION:

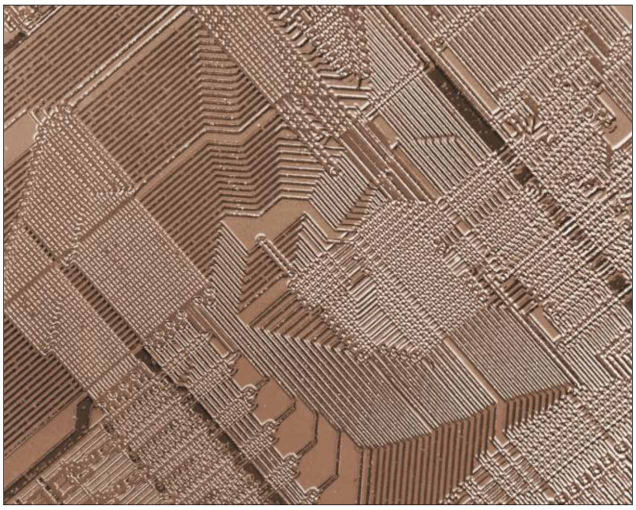
What are the grain size and boundary characteristics of Cu-interconnects on the sub-micron scale?

### Introduction

The microelectronics industry is continuing to push towards smaller and smaller devices, edging into the realms of nanotechnology. This has been stimulated by the demand for higher operating frequencies, greater circuit complexity, miniaturisation and lower power consumption. As gate lengths approach 0.25 µm and below, there is a demand for interconnect line widths to decrease and the number of levels of interconnects to increase. However, this can cause some serious problems – narrower lines suffer from higher resistivity, while closer spacing of the lines increases the capacitance. In response to these drawbacks, one of the key recent developments has been the switch from aluminium-based to copper-based interconnects, as copper has a significantly lower resistance.

But, as with aluminium, failure due to electromigration remains a major reliability concern in copper interconnects. Electromigration is the current-induced diffusion of atoms due to the momentum transfer of moving electrons; this may lead to the undesired formation of voids and hillocks, both of which can cause open and short circuit failures. The potential failure of interconnects, and hence their lifetimes, is strongly dependent on key microstructural parameters such as grain size, grain shape, grain boundary characteristics and texture.

High resolution EBSD gives researchers the capability to measure these critical parameters, even on the ultra-narrow interconnects that are currently in development. Although EBSD analyses on this scale have been reported before, typically they have been on heavier materials, such as platinum thin films. The key to this investigation is that high resolution EBSD data have been acquired from copper lines in an insulating matrix, without the need for any conductive coating (to remove any charge build up). This is only possible because the high sensitivity of the Nordlys detector allows analysis at very high speeds (e.g. >50 points / s) with small probe currents (≤1 nA). After EBSD analysis the sample can be returned to testing or even production.



This application focuses on the significance of grain and boundary characteristics in 500 nm wide copper lines produced by the Damascene process.

### Analysis details

**Experimental set up**

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|---|
| Sample preparation: Brief ion beam milling |
| SEM type: LEO Supra 55VP (FEG SEM) |
| EBSD System: HKL CHANNEL 5 with Nordlys II detector |
| Acc V: 20 kV |
| Probe Current: 1 nA |
| Working distance: 5 mm |

**EBSD details**

| | High resolution | Ultra-high resolution |
|---|---|---|
| Grid dimensions: | 537 x 770 | 395x385 |
| Grid spacing: | 20nm | 5 nm |
| Number of points: | 413,490 | 152,075 |
| Mapping speed: | 50 patterns / s | 50 patterns / s |
| Noise filtering level: | Low | Low |

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## Results

### 1. High Resolution Analysis

**Figure 1 – Orientation Map:**
This EBSD map shows the orientation (using the all-Euler colouring scheme) superimposed on an EBSP quality map. The high angle grain boundaries (> 10° misorientation) are shown in black, with Σ3 twin boundaries (60° rotation about <111>) shown in red. The spacing between each measurement is 20 nm. The microstructure of the copper interconnect lines is dominated by the abundance of twin boundaries. These make up 78.6% of all the boundaries over 10° in this area. Such an abundance of twins may have a significant benefit on the electrical properties and the lifetime of the lines. This is for two reasons: firstly because twin boundaries have a relatively low mobility, resulting in a high degree of microstructural stability, and secondly because twins have a much lower electrical resistance compared to other incoherent high angle boundaries. The yellow box in the map marks the area of the ultra-high resolution analysis (see figure 5).

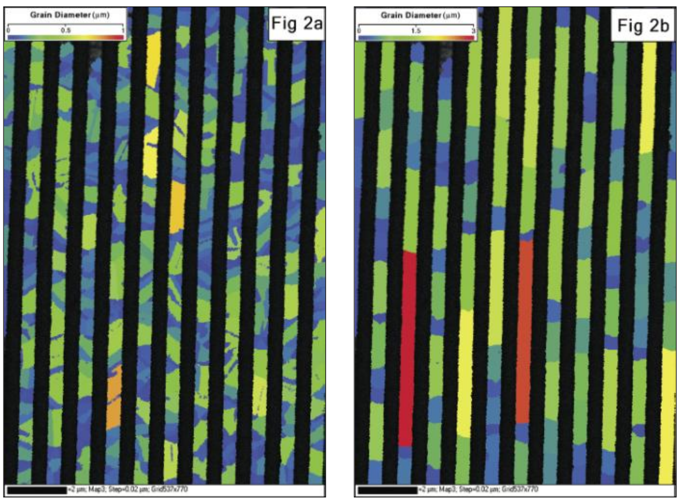


**Figure 2 – Grain Size Maps:**
(a) This figure shows the grain size distribution in the Cu-interconnect lines. All high angle boundaries (including twins) are treated as grain boundaries, so individual twin domains are measured as whole grains. The average grain size is measured at 0.28 μm. (b) This figure shows the grain size distribution in the Cu-interconnect lines, with twin boundaries excluded from the measurement process. The average grain size is now measured at 0.71 μm.
As mentioned earlier, the twin boundaries have low mobility and resistance and therefore may not have a large influence on the electrical properties of the interconnects. Excluding these twin boundaries reveals a “bamboo structure”, which is considered beneficial to the electrical properties. It also highlights the position of “random” high angle boundaries (i.e. nontwins), which may be the source of defects during electromigration.

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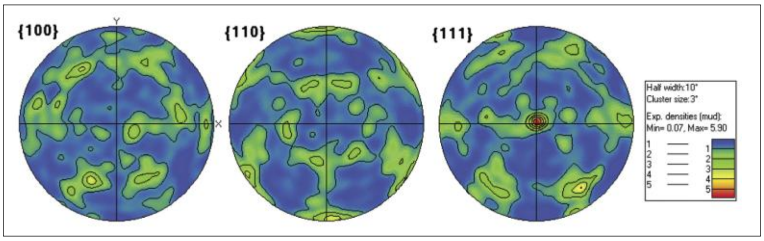


**Figure 3 – Texture:**
The pole figures show that these Cu-interconnect lines are also highly textured, with the <111> pole parallel to the normal direction. However, this is not a true fibre texture as the in-plane texture is also quite strong, with the <110> direction oriented parallel to the length of the Cu-interconnect lines (the Y direction in the pole figures). The contours mark 1, 2, 3, 4, 5 x uniform density.

## 2. Ultra-High Resolution Analysis

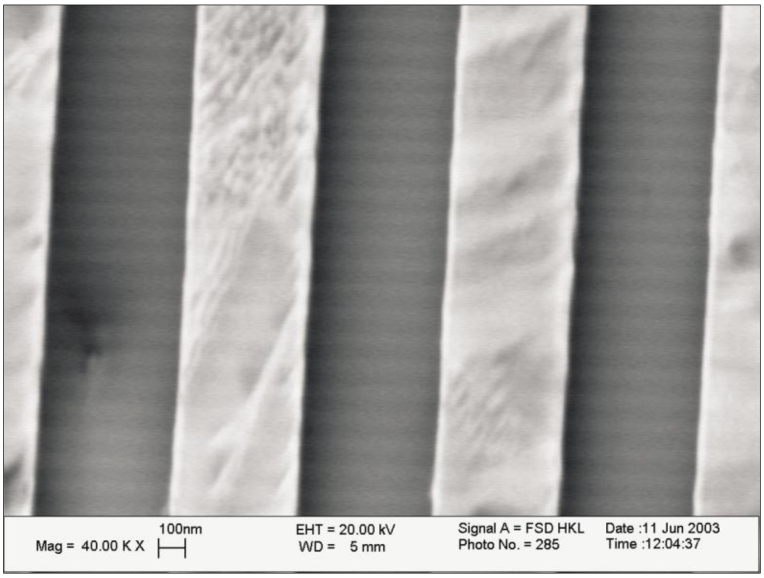


**Figure 4 – Forescatter image:**
This is a forescatter image taken at high magnification, showing the area highlighted in figure 1. The orientation contrast is relatively weak, but even so, some grain and twin structures can be resolved. Compare this image with the EBSD maps of the same area shown in figure 5. The scale bar marks 100 nm.

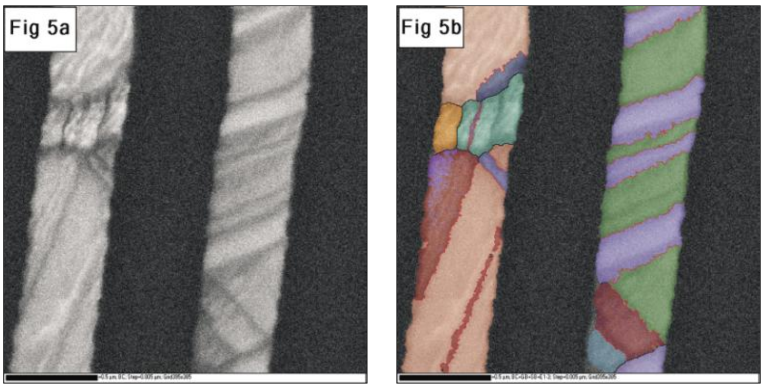


**Figure 5 – EBSD Maps:**
(a) EBSP quality map: this shows the variations in the quality of the diffraction patterns across the 2 lines imaged in figure 4. Where the electron beam hits a grain boundary or a twin boundary, the diffraction pattern quality decreases and the boundary appears as a darker line in the EBSP quality map. The spacing between each measurement is 5 nm.
(b) Orientation Map, superimposed on the EBSP quality map: here the orientations are coloured using the all-Euler colouring scheme, with $\Sigma 3$ twins marked in red and other high angle boundaries in black.. A very short working distance of 5mm was used during data collection in the SEM, allowing acquisition of such high resolution data. In this map very fine twin domains (< 30 nm wide) can be identified, many of which were not resolved in the lower resolution map shown in figure 1. These fine twin boundaries may be important for identifying the source of defects in the Cu-interconnect lines, as it is possible that they may act as barriers to other boundaries during growth, leading to the initiation of points of failure.

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## Conclusion

With the development of smaller and smaller interconnects in the microelectronics industry, grain and boundary features on the scale of 10s – 100s of nanometres become critical for the optimisation of device properties. In this study such nano-structures in Cu-interconnect lines have been resolved, using ultra-high spatial resolution EBSD. The unique combination of spatial and crystallographic information provided by EBSD analyses makes it the ideal technique for assessing interconnect microstructures. In this example, the dominance of twin boundaries results in a bamboo structure in the lines although, on the very small scale, twins may be acting as barriers to other high angle boundaries during growth. These fine structures would have been difficult to identify using other techniques, and they may hold the key to finding the source of defects in Cu-interconnect lines.

**ANSWER:**

There is a very high abundance of Σ3 twin boundaries, resulting in a beneficial bamboo structure in these interconnect lines.

**Acknowledgements**

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